

Spartan-3A and Spartan-3A DSP Libraries Guide for Schematic Designs

ISE 10.1

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About this Guide

This guide is part of the ISE documentation collection and covers the use of Xilinx design elements in schematics. A separate version of this guide is also available if you prefer to work with Verilog or VHDL in your circuit design activities.

This guide contains the following:

- A general introduction to the design elements, including descriptions of the types of elements available in this architecture.
- A list of pre-existing design elements are automatically changed by the ISE software tools when they are used in this architecture, thus ensuring that you are always able to take full advantage of the latest circuit design advances.
- A list of the design elements that are supported in this architecture, organized by functional categories. Click on the element of your choice to immediately access its profile.
- Individual profiles describing each of the primitives and macros, and including, as appropriate, for each element:
 - Its formal name
 - A brief introduction to each element, including the names of all architectures in which it is supported
 - Its schematic symbol
 - Logic tables (if any)
 - Port descriptions (if any)
 - A list of available attributes
 - References to any additional sources of information

About this Architecture

This version of the Libraries Guide describes the categories of design elements that comprise the Xilinx Unified Libraries for this architecture. These categories are:

- **Primitives** - The simplest design elements in the Xilinx libraries. Primitives are the design element "atoms." Primitives can be created from primitives or macros. Examples of Xilinx primitives are the simple buffer, BUF, and the D flip-flop with clock enable and clear, FDCE.
- **Macros** - The design element "molecules" of the Xilinx libraries. Macros can be created from the design element primitives or macros. For example, the FD4CE flip-flop macro is a composite of 4 FDCE primitives.

Xilinx maintains software libraries with hundreds of functional design elements (unimacros and primitives) for different device architectures. New functional elements are assembled with each release of development system software. In addition to a comprehensive Unified Library containing all design elements, this guide is one in a series of architecture-specific libraries.

Design Element Retargeting

To ensure that Xilinx customers are able to take full advantage of the latest circuit design advances, certain design elements are automatically changed by the ISE software tools when they are used in this architecture.

The following table lists these elements and the more advanced elements into which they are transformed.

Original Element	Modern Equivalent
BUFGCE_1	BUFGCE + INV
BUFGDLL	DCM_SP + BUFG
BUFGMUX_1	BUFGMUX + INV
BUFGP	BUFG
CAPTURE_SPARTAN3	CAPTURE_SPARTAN3a
CLKDLL	DCM_SP
CLKDLLE	DCM_SP
CLKDLLHF	DCM_SP
FD	FDCPE
FD_1	FDCPE + INV
FDC	FDCPE
FDC_1	FDCPE + INV
FDCE	FDCPE
FDCE_1	FDCPE + INV
FDCP	FDCPE
FDCP_1	FDCPE + INV
FDE	FDCPE
FDE_1	FDCPE + INV
FDPE	FDCPE
FDPE_1	FDCPE + INV
FDR	FDRSE
FDR_1	FDRSE + INV
FDRE	FDRSE
FDRE_1	FDRSE + INV
FDRS	FDRSE
FDRS_1	FDRSE + INV
FDS	FDRSE
FDS_1	FDRSE + INV
FDSE	FDRSE
FDSE_1	FDRSE + INV
LD	LDCPE
LD_1	LDCPE + INV
LDC	LDCPE

Original Element	Modern Equivalent
LDC_1	LDCPE + INV
LDCE	LDCPE
LDCE_1	LDCPE + INV
LDE	LDCPE
LDE_1	LDCPE + INV
LDP	LDCPE
LDP_1	LDCPE + INV
LDPE	LDCPE
LDPE_1	LDCPE + INV
RAM128X1S_1	RAM128x1s + INV on clock
RAM16X1D_1	RAM16X1D + INV on clock
RAM16X1S_1	RAM16X1S + INV on clock
RAM16X2S	2=RAM16x1s
RAM16X4S	4=RAM16x1s
RAM16X8S	8=RAM16x1s
RAM32X1D_1	RAM32x1d + INV on clock
RAM32X1S_1	RAM32x1s + INV on clock
RAM32X2S	2 RAM32x1s
RAM32X4S	4 RAM32x1s
RAM32X8S	8 RAM32x1s
RAM64X1S_1	RAM64x1s + INV on clock
RAM64X2S	2 RAM64x1s
RAMB16_S1_S1	RAMB16BWE
RAMB16_S1_S18	RAMB16BWE
RAMB16_S1_S2	RAMB16BWE
RAMB16_S1_S36	RAMB16BWE
RAMB16_S1_S4	RAMB16BWE
RAMB16_S1_S9	RAMB16BWE
RAMB16_S1	RAMB16BWE
RAMB16_S18_S18	RAMB16BWE
RAMB16_S18_S36	RAMB16BWE
RAMB16_S18	RAMB16BWE
RAMB16_S2_S18	RAMB16BWE
RAMB16_S2_S2	RAMB16BWE
RAMB16_S2_S36	RAMB16BWE
RAMB16_S2_S4	RAMB16BWE
RAMB16_S2_S9	RAMB16BWE
RAMB16_S2	RAMB16BWE

Original Element	Modern Equivalent
RAMB16_S36_S36	RAMB16BWE
RAMB16_S36	RAMB16BWE
RAMB16_S4_S18	RAMB16BWE
RAMB16_S4_S36	RAMB16BWE
RAMB16_S4_S4	RAMB16BWE
RAMB16_S4_S9	RAMB16BWE
RAMB16_S4	RAMB16BWE
RAMB16_S9_S18	RAMB16BWE
RAMB16_S9_S36	RAMB16BWE
RAMB16_S9_S9	RAMB16BWE
RAMB16_S9	RAMB16BWE
RAMB4_S1_S1	RAMB16BWE
RAMB4_S1_S16	RAMB16BWE
RAMB4_S1_S2	RAMB16BWE
RAMB4_S1_S4	RAMB16BWE
RAMB4_S1_S8	RAMB16BWE
RAMB4_S1	RAMB16BWE
RAMB4_S16_S16	RAMB16BWE
RAMB4_S16	RAMB16BWE
RAMB4_S2_S16	RAMB16BWE
RAMB4_S2_S2	RAMB16BWE
RAMB4_S2_S4	RAMB16BWE
RAMB4_S2_S8	RAMB16BWE
RAMB4_S2	RAMB16BWE
RAMB4_S4_S16	RAMB16BWE
RAMB4_S4_S4	RAMB16BWE
RAMB4_S4_S8	RAMB16BWE
RAMB4_S4	RAMB16BWE
RAMB4_S8_S16	RAMB16BWE
RAMB4_S8_S8	RAMB16BWE
STARTUP_SPARTAN3	STARTUP_SPARTAN3a

Functional Categories

This section categorizes, by function, the circuit design elements described in detail later in this guide. The elements (*primitives* and *macros*) are listed in alphanumeric order under each functional category.

Arithmetic	Decoder	Latch
Buffer	Flip Flop	Logic
Carry Logic	General	LUT
Comparator	IO	Memory
Counter	IO FlipFlop	Mux
DDR Flip Flop	IO Latch	Shift Register

Arithmetic

Design Element	Description
ACC16	Macro: 16-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset
ACC4	Macro: 4-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset
ACC8	Macro: 8-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset
ADD16	Macro: 16-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow
ADD4	Macro: 4-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow
ADD8	Macro: 8-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow
ADSU16	Macro: 16-Bit Cascadable Adder/Subtractor with Carry-In, Carry-Out, and Overflow
ADSU4	Macro: 4-Bit Cascadable Adder/Subtractor with Carry-In, Carry-Out, and Overflow
ADSU8	Macro: 8-Bit Cascadable Adder/Subtractor with Carry-In, Carry-Out, and Overflow
DSP48A	Primitive: Multi-Functional, Cascadable, 48-bit Output, Arithmetic Block
MULT18X18SIO	Primitive: 18 x 18 Cascadable Signed Multiplier with Optional Input and Output Registers, Clock Enable, and Synchronous Reset

Buffer

Design Element	Description
BUF	Primitive: General Purpose Buffer
BUFCF	Primitive: Fast Connect Buffer
BUFG	Primitive: Global Clock Buffer
BUFGCE	Primitive: Global Clock Buffer with Clock Enable
BUFGMUX	Primitive: Global Clock MUX Buffer

Carry Logic

Design Element	Description
MUXCY	Primitive: 2-to-1 Multiplexer for Carry Logic with General Output
MUXCY_D	Primitive: 2-to-1 Multiplexer for Carry Logic with Dual Output
MUXCY_L	Primitive: 2-to-1 Multiplexer for Carry Logic with Local Output
XORCY	Primitive: XOR for Carry Logic with General Output
XORCY_D	Primitive: XOR for Carry Logic with Dual Output
XORCY_L	Primitive: XOR for Carry Logic with Local Output

Comparator

Design Element	Description
COMP16	Macro: 16-Bit Identity Comparator
COMP2	Macro: 2-Bit Identity Comparator
COMP4	Macro: 4-Bit Identity Comparator
COMP8	Macro: 8-Bit Identity Comparator
COMPM16	Macro: 16-Bit Magnitude Comparator
COMPM2	Macro: 2-Bit Magnitude Comparator
COMPM4	Macro: 4-Bit Magnitude Comparator
COMPM8	Macro: 8-Bit Magnitude Comparator
COMPMC16	Macro: 16-Bit Magnitude Comparator
COMPMC8	Macro: 8-Bit Magnitude Comparator

Counter

Design Element	Description
CB16CE	Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CB16CLE	Macro: 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear
CB16CLED	Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear
CB16RE	Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CB2CE	Macro: 2-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CB2CLE	Macro: 2-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear
CB2CLED	Macro: 2-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear
CB2RE	Macro: 2-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CB4CE	Macro: 4-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CB4CLE	Macro: 4-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear

Design Element	Description
CB4CLED	Macro: 4-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear
CB4RE	Macro: 4-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CB8CE	Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CB8CLE	Macro: 8-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear
CB8CLED	Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear
CB8RE	Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CC16CE	Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CC16CLE	Macro: 16-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CC16CLED	Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear
CC16RE	Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CC8CE	Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CC8CLE	Macro: 8-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear
CC8CLED	Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear
CC8RE	Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset
CD4CE	Macro: 4-Bit Cascadable BCD Counter with Clock Enable and Asynchronous Clear
CD4CLE	Macro: 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Asynchronous Clear
CD4RE	Macro: 4-Bit Cascadable BCD Counter with Clock Enable and Synchronous Reset
CD4RLE	Macro: 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Synchronous Reset
CJ4CE	Macro: 4-Bit Johnson Counter with Clock Enable and Asynchronous Clear
CJ4RE	Macro: 4-Bit Johnson Counter with Clock Enable and Synchronous Reset
CJ5CE	Macro: 5-Bit Johnson Counter with Clock Enable and Asynchronous Clear
CJ5RE	Macro: 5-Bit Johnson Counter with Clock Enable and Synchronous Reset
CJ8CE	Macro: 8-Bit Johnson Counter with Clock Enable and Asynchronous Clear
CJ8RE	Macro: 8-Bit Johnson Counter with Clock Enable and Synchronous Reset
CR16CE	Macro: 16-Bit Negative-Edge Binary Ripple Counter with Clock Enable and Asynchronous Clear
CR8CE	Macro: 8-Bit Negative-Edge Binary Ripple Counter with Clock Enable and Asynchronous Clear

DDR Flip Flop

Design Element	Description
IDDR2	Primitive: Double Data Rate Input D Flip-Flop with Optional Data Alignment, Clock Enable and Programmable Synchronous or Asynchronous Set/Reset
ODDR2	Primitive: Dual Data Rate Output D Flip-Flop with Optional Data Alignment, Clock Enable and Programmable Synchronous or Asynchronous Set/Reset

Decoder

Design Element	Description
D2_4E	Macro: 2- to 4-Line Decoder/Demultiplexer with Enable
D3_8E	Macro: 3- to 8-Line Decoder/Demultiplexer with Enable
D4_16E	Macro: 4- to 16-Line Decoder/Demultiplexer with Enable
DEC_CC16	Macro: 16-Bit Active Low Decoder
DEC_CC4	Macro: 4-Bit Active Low Decoder
DEC_CC8	Macro: 8-Bit Active Low Decoder
DECODE16	Macro: 16-Bit Active-Low Decoder
DECODE32	Macro: 32-Bit Active-Low Decoder
DECODE4	Macro: 4-Bit Active-Low Decoder
DECODE64	Macro: 64-Bit Active-Low Decoder
DECODE8	Macro: 8-Bit Active-Low Decoder

Flip Flop

Design Element	Description
FD16CE	Macro: 16-Bit Data Register with Clock Enable and Asynchronous Clear
FD16RE	Macro: 16-Bit Data Register with Clock Enable and Synchronous Reset
FD4CE	Macro: 4-Bit Data Register with Clock Enable and Asynchronous Clear
FD4RE	Macro: 4-Bit Data Register with Clock Enable and Synchronous Reset
FD8CE	Macro: 8-Bit Data Register with Clock Enable and Asynchronous Clear
FD8RE	Macro: 8-Bit Data Register with Clock Enable and Synchronous Reset
FDCPE	Primitive: D Flip-Flop with Clock Enable and Asynchronous Preset and Clear
FDCPE_1	Primitive: D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Preset and Clear
FDP	Primitive: D Flip-Flop with Asynchronous Preset
FDP_1	Primitive: D Flip-Flop with Negative-Edge Clock and Asynchronous Preset
FDRSE	Primitive: D Flip-Flop with Synchronous Reset and Set and Clock Enable
FDRSE_1	Primitive: D Flip-Flop with Negative-Clock Edge, Synchronous Reset and Set, and Clock Enable
FJKC	Macro: J-K Flip-Flop with Asynchronous Clear
FJKCE	Macro: J-K Flip-Flop with Clock Enable and Asynchronous Clear

Design Element	Description
FJKP	Macro: J-K Flip-Flop with Asynchronous Preset
FJKPE	Macro: J-K Flip-Flop with Clock Enable and Asynchronous Preset
FJKRSE	Macro: J-K Flip-Flop with Clock Enable and Synchronous Reset and Set
FJKSRE	Macro: J-K Flip-Flop with Clock Enable and Synchronous Set and Reset
FTC	Macro: Toggle Flip-Flop with Asynchronous Clear
FTCE	Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Clear
FTCLE	Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear
FTCLEX	Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear
FTP	Macro: Toggle Flip-Flop with Asynchronous Preset
FTPE	Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Preset
FTPLE	Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Preset
FTRSE	Macro: Toggle Flip-Flop with Clock Enable and Synchronous Reset and Set
FTRSLE	Macro: Toggle/Loadable Flip-Flop with Clock Enable and Synchronous Reset and Set
FTSRE	Macro: Toggle Flip-Flop with Clock Enable and Synchronous Set and Reset
FTSRLE	Macro: Toggle/Loadable Flip-Flop with Clock Enable and Synchronous Set and Reset

General

Design Element	Description
BSCAN_SPARTAN3A	Primitive: Spartan-3A Global Set/Reset, Global 3-State and Configuration Start-Up Clock Interface
CAPTURE_SPARTAN3A	Primitive: Spartan-3A Register State Capture for Bitstream Readback
DCM_SP	Primitive: Digital Clock Manager
DNA_PORT	Primitive: Device DNA Data Access Port
GND	Primitive: Ground-Connection Signal Tag
ICAP_SPARTAN3A	Primitive: Internal Configuration Access Port
KEEPER	Primitive: KEEPER Symbol
PULLDOWN	Primitive: Resistor to GND for Input Pads, Open-Drain, and 3-State Outputs
PULLUP	Primitive: Resistor to VCC for Input PADS, Open-Drain, and 3-State Outputs
SPI_ACCESS	Primitive: Internal Logic Access to the Serial Peripheral Interface (SPI) PROM Data
STARTUP_SPARTAN3A	Primitive: Spartan-3A Global Set/Reset, Global 3-State and Configuration Start-Up Clock Interface
VCC	Primitive: VCC-Connection Signal Tag

IO

Design Element	Description
IBUF	Primitive: Input Buffer
IBUF_DLY_ADJ	Primitive: Dynamically Adjustable Input Delay Buffer

Design Element	Description
IBUF16	Macro: 16-Bit Input Buffer
IBUF4	Macro: 4-Bit Input Buffer
IBUF8	Macro: 8-Bit Input Buffer
IBUFDS	Primitive: Differential Signaling Input Buffer with Optional Delay
IBUFDS_DLY_ADJ	Primitive: Dynamically Adjustable Differential Input Delay Buffer
IBUFG	Primitive: Dedicated Input Clock Buffer
IBUFGDS	Primitive: Differential Signaling Dedicated Input Clock Buffer and Optional Delay
IOBUF	Primitive: Bi-Directional Buffer
IOBUFDS	Primitive: 3-State Differential Signaling I/O Buffer with Active Low Output Enable
OBUF	Primitive: Output Buffer
OBUF16	Macro: 16-Bit Output Buffer
OBUF4	Macro: 4-Bit Output Buffer
OBUF8	Macro: 8-Bit Output Buffer
OBUFDS	Primitive: Differential Signaling Output Buffer
OBUFT	Primitive: 3-State Output Buffer with Active Low Output Enable
OBUFT16	Macro: 16-Bit 3-State Output Buffer with Active Low Output Enable
OBUFT4	Macro: 4-Bit 3-State Output Buffers with Active-Low Output Enable
OBUFT8	Macro: 8-Bit 3-State Output Buffers with Active-Low Output Enable
OBUFTDS	Primitive: 3-State Output Buffer with Differential Signaling, Active-Low Output Enable

IO FlipFlop

Design Element	Description
IFD	Macro: Input D Flip-Flop
IFD_1	Macro: Input D Flip-Flop with Inverted Clock (Asynchronous Preset)
IFD16	Macro: 16-Bit Input D Flip-Flop
IFD4	Macro: 4-Bit Input D Flip-Flop
IFD8	Macro: 8-Bit Input D Flip-Flop
IFDI	Macro: Input D Flip-Flop (Asynchronous Preset)
IFDI_1	Macro: Input D Flip-Flop with Inverted Clock (Asynchronous Preset)
IFDX	Macro: Input D Flip-Flop with Clock Enable
IFDX_1	Macro: Input D Flip-Flop with Inverted Clock and Clock Enable
IFDX16	Macro: 16-Bit Input D Flip-Flops with Clock Enable
IFDX4	Macro: 4-Bit Input D Flip-Flop with Clock Enable
IFDX8	Macro: 8-Bit Input D Flip-Flop with Clock Enable
IFDXI	Macro: Input D Flip-Flop with Clock Enable (Asynchronous Preset)
IFDXI_1	Macro: Input D Flip-Flop with Inverted Clock and Clock Enable (Asynchronous Preset)
OFD	Macro: Output D Flip-Flop

Design Element	Description
OFD_1	Macro: Output D Flip-Flop with Inverted Clock
OFD16	Macro: 16-Bit Output D Flip-Flop
OFD4	Macro: 4-Bit Output D Flip-Flop
OFD8	Macro: 8-Bit Output D Flip-Flop
OFDE	Macro: D Flip-Flop with Active-High Enable Output Buffers
OFDE_1	Macro: D Flip-Flop with Active-High Enable Output Buffer and Inverted Clock
OFDE16	Macro: 16-Bit D Flip-Flop with Active-High Enable Output Buffers
OFDE4	Macro: 4-Bit D Flip-Flop with Active-High Enable Output Buffers
OFDE8	Macro: 8-Bit D Flip-Flop with Active-High Enable Output Buffers
OFDI	Macro: Output D Flip-Flop (Asynchronous Preset)
OFDI_1	Macro: Output D Flip-Flop with Inverted Clock (Asynchronous Preset)
OFDT	Macro: D Flip-Flop with Active-Low 3-State Output Buffer
OFDT_1	Macro: D Flip-Flop with Active-Low 3-State Output Buffer and Inverted Clock
OFDT16	Macro: 16-Bit D Flip-Flop with Active-Low 3-State Output Buffers
OFDT4	Macro: 4-Bit D Flip-Flop with Active-Low 3-State Output Buffers
OFDT8	Macro: 8-Bit D Flip-Flop with Active-Low 3-State Output Buffers
OFDX	Macro: Output D Flip-Flop with Clock Enable
OFDX_1	Macro: Output D Flip-Flop with Inverted Clock and Clock Enable
OFDX16	Macro: 16-Bit Output D Flip-Flop with Clock Enable
OFDX4	Macro: 4-Bit Output D Flip-Flop with Clock Enable
OFDX8	Macro: 8-Bit Output D Flip-Flop with Clock Enable
OFDXI	Macro: Output D Flip-Flop with Clock Enable (Asynchronous Preset)
OFDXI_1	Macro: Output D Flip-Flop with Inverted Clock and Clock Enable (Asynchronous Preset)

IO Latch

Design Element	Description
ILD	Macro: Transparent Input Data Latch
ILD_1	Macro: Transparent Input Data Latch with Inverted Gate
ILD16	Macro: Transparent Input Data Latch
ILD4	Macro: Transparent Input Data Latch
ILD8	Macro: Transparent Input Data Latch
ILDI	Macro: Transparent Input Data Latch (Asynchronous Preset)
ILDI_1	Macro: Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)
ILDY	Macro: Transparent Input Data Latch
ILDY_1	Macro: Transparent Input Data Latch with Inverted Gate
ILDY16	Macro: Transparent Input Data Latch
ILDY4	Macro: Transparent Input Data Latch

Design Element	Description
ILD8	Macro: Transparent Input Data Latch
ILD8I	Macro: Transparent Input Data Latch (Asynchronous Preset)
ILD8I_1	Macro: Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)

Latch

Design Element	Description
LD16	Macro: Multiple Transparent Data Latch
LD16CE	Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable
LD4	Macro: Multiple Transparent Data Latch
LD4CE	Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable
LD8	Macro: Multiple Transparent Data Latch
LD8CE	Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable
LDCP	Primitive: Transparent Data Latch with Asynchronous Clear and Preset
LDCP_1	Primitive: Transparent Data Latch with Asynchronous Clear and Preset and Inverted Gate
LDCPE	Primitive: Transparent Data Latch with Asynchronous Clear and Preset and Gate Enable
LDCPE_1	Primitive: Transparent Data Latch with Asynchronous Clear and Preset, Gate Enable, and Inverted Gate

Logic

Design Element	Description
AND12	Macro: 12- Input AND Gate with Non-Inverted Inputs
AND16	Macro: 16- Input AND Gate with Non-Inverted Inputs
AND2	Primitive: 2-Input AND Gate with Non-Inverted Inputs
AND2B1	Primitive: 2-Input AND Gate with 1 Inverted and 1 Non-Inverted Inputs
AND2B2	Primitive: 2-Input AND Gate with Inverted Inputs
AND3	Primitive: 3-Input AND Gate with Non-Inverted Inputs
AND3B1	Primitive: 3-Input AND Gate with 1 Inverted and 2 Non-Inverted Inputs
AND3B2	Primitive: 3-Input AND Gate with 2 Inverted and 1 Non-Inverted Inputs
AND3B3	Primitive: 3-Input AND Gate with Inverted Inputs
AND4	Primitive: 4-Input AND Gate with Non-Inverted Inputs
AND4B1	Primitive: 4-Input AND Gate with 1 Inverted and 3 Non-Inverted Inputs
AND4B2	Primitive: 4-Input AND Gate with 2 Inverted and 2 Non-Inverted Inputs
AND4B3	Primitive: 4-Input AND Gate with 3 Inverted and 1 Non-Inverted Inputs
AND4B4	Primitive: 4-Input AND Gate with Inverted Inputs
AND5	Primitive: 5-Input AND Gate with Non-Inverted Inputs
AND5B1	Primitive: 5-Input AND Gate with 1 Inverted and 4 Non-Inverted Inputs

Design Element	Description
AND5B2	Primitive: 5-Input AND Gate with 2 Inverted and 3 Non-Inverted Inputs
AND5B3	Primitive: 5-Input AND Gate with 3 Inverted and 2 Non-Inverted Inputs
AND5B4	Primitive: 5-Input AND Gate with 4 Inverted and 1 Non-Inverted Inputs
AND5B5	Primitive: 5-Input AND Gate with Inverted Inputs
AND6	Macro: 6-Input AND Gate with Non-Inverted Inputs
AND7	Macro: 7-Input AND Gate with Non-Inverted Inputs
AND8	Macro: 8-Input AND Gate with Non-Inverted Inputs
AND9	Macro: 9-Input AND Gate with Non-Inverted Inputs
INV	Primitive: Inverter
INV16	Macro: 16 Inverters
INV4	Macro: Four Inverters
INV8	Macro: Eight Inverters
MULT_AND	Primitive: Fast Multiplier AND
NAND12	Macro: 12- Input NAND Gate with Non-Inverted Inputs
NAND16	Macro: 16- Input NAND Gate with Non-Inverted Inputs
NAND2	Primitive: 2-Input NAND Gate with Non-Inverted Inputs
NAND2B1	Primitive: 2-Input NAND Gate with 1 Inverted and 1 Non-Inverted Inputs
NAND2B2	Primitive: 2-Input NAND Gate with Inverted Inputs
NAND3	Primitive: 3-Input NAND Gate with Non-Inverted Inputs
NAND3B1	Primitive: 3-Input NAND Gate with 1 Inverted and 2 Non-Inverted Inputs
NAND3B2	Primitive: 3-Input NAND Gate with 2 Inverted and 1 Non-Inverted Inputs
NAND3B3	Primitive: 3-Input NAND Gate with Inverted Inputs
NAND4	Primitive: 4-Input NAND Gate with Non-Inverted Inputs
NAND4B1	Primitive: 4-Input NAND Gate with 1 Inverted and 3 Non-Inverted Inputs
NAND4B2	Primitive: 4-Input NAND Gate with 2 Inverted and 2 Non-Inverted Inputs
NAND4B3	Primitive: 4-Input NAND Gate with 3 Inverted and 1 Non-Inverted Inputs
NAND4B4	Primitive: 4-Input NAND Gate with Inverted Inputs
NAND5	Primitive: 5-Input NAND Gate with Non-Inverted Inputs
NAND5B1	Primitive: 5-Input NAND Gate with 1 Inverted and 4 Non-Inverted Inputs
NAND5B2	Primitive: 5-Input NAND Gate with 2 Inverted and 3 Non-Inverted Inputs
NAND5B3	Primitive: 5-Input NAND Gate with 3 Inverted and 2 Non-Inverted Inputs
NAND5B4	Primitive: 5-Input NAND Gate with 4 Inverted and 1 Non-Inverted Inputs
NAND5B5	Primitive: 5-Input NAND Gate with Inverted Inputs
NAND6	Macro: 6-Input NAND Gate with Non-Inverted Inputs
NAND7	Macro: 7-Input NAND Gate with Non-Inverted Inputs
NAND8	Macro: 8-Input NAND Gate with Non-Inverted Inputs
NAND9	Macro: 9-Input NAND Gate with Non-Inverted Inputs
NOR12	Macro: 12-Input NOR Gate with Non-Inverted Inputs

Design Element	Description
NOR16	Macro: 16-Input NOR Gate with Non-Inverted Inputs
NOR2	Primitive: 2-Input NOR Gate with Non-Inverted Inputs
NOR2B1	Primitive: 2-Input NOR Gate with 1 Inverted and 1 Non-Inverted Inputs
NOR2B2	Primitive: 2-Input NOR Gate with Inverted Inputs
NOR3	Primitive: 3-Input NOR Gate with Non-Inverted Inputs
NOR3B1	Primitive: 3-Input NOR Gate with 1 Inverted and 2 Non-Inverted Inputs
NOR3B2	Primitive: 3-Input NOR Gate with 2 Inverted and 1 Non-Inverted Inputs
NOR3B3	Primitive: 3-Input NOR Gate with Inverted Inputs
NOR4	Primitive: 4-Input NOR Gate with Non-Inverted Inputs
NOR4B1	Primitive: 4-Input NOR Gate with 1 Inverted and 3 Non-Inverted Inputs
NOR4B2	Primitive: 4-Input NOR Gate with 2 Inverted and 2 Non-Inverted Inputs
NOR4B3	Primitive: 4-Input NOR Gate with 3 Inverted and 1 Non-Inverted Inputs
NOR4B4	Primitive: 4-Input NOR Gate with Inverted Inputs
NOR5	Primitive: 5-Input NOR Gate with Non-Inverted Inputs
NOR5B1	Primitive: 5-Input NOR Gate with 1 Inverted and 4 Non-Inverted Inputs
NOR5B2	Primitive: 5-Input NOR Gate with 2 Inverted and 3 Non-Inverted Inputs
NOR5B3	Primitive: 5-Input NOR Gate with 3 Inverted and 2 Non-Inverted Inputs
NOR5B4	Primitive: 5-Input NOR Gate with 4 Inverted and 1 Non-Inverted Inputs
NOR5B5	Primitive: 5-Input NOR Gate with Inverted Inputs
NOR6	Macro: 6-Input NOR Gate with Non-Inverted Inputs
NOR7	Macro: 7-Input NOR Gate with Non-Inverted Inputs
NOR8	Macro: 8-Input NOR Gate with Non-Inverted Inputs
NOR9	Macro: 9-Input NOR Gate with Non-Inverted Inputs
OR12	Macro: 12-Input OR Gate with Non-Inverted Inputs
OR16	Macro: 16-Input OR Gate with Non-Inverted Inputs
OR2	Primitive: 2-Input OR Gate with Non-Inverted Inputs
OR2B1	Primitive: 2-Input OR Gate with 1 Inverted and 1 Non-Inverted Inputs
OR2B2	Primitive: 2-Input OR Gate with Inverted Inputs
OR3	Primitive: 3-Input OR Gate with Non-Inverted Inputs
OR3B1	Primitive: 3-Input OR Gate with 1 Inverted and 2 Non-Inverted Inputs
OR3B2	Primitive: 3-Input OR Gate with 2 Inverted and 1 Non-Inverted Inputs
OR3B3	Primitive: 3-Input OR Gate with Inverted Inputs
OR4	Primitive: 4-Input OR Gate with Non-Inverted Inputs
OR4B1	Primitive: 4-Input OR Gate with 1 Inverted and 3 Non-Inverted Inputs
OR4B2	Primitive: 4-Input OR Gate with 2 Inverted and 2 Non-Inverted Inputs
OR4B3	Primitive: 4-Input OR Gate with 3 Inverted and 1 Non-Inverted Inputs
OR4B4	Primitive: 4-Input OR Gate with Inverted Inputs
OR5	Primitive: 5-Input OR Gate with Non-Inverted Inputs

Design Element	Description
OR5B1	Primitive: 5-Input OR Gate with 1 Inverted and 4 Non-Inverted Inputs
OR5B2	Primitive: 5-Input OR Gate with 2 Inverted and 3 Non-Inverted Inputs
OR5B3	Primitive: 5-Input OR Gate with 3 Inverted and 2 Non-Inverted Inputs
OR5B4	Primitive: 5-Input OR Gate with 4 Inverted and 1 Non-Inverted Inputs
OR5B5	Primitive: 5-Input OR Gate with Inverted Inputs
OR6	Macro: 6-Input OR Gate with Non-Inverted Inputs
OR7	Macro: 7-Input OR Gate with Non-Inverted Inputs
OR8	Macro: 8-Input OR Gate with Non-Inverted Inputs
OR9	Macro: 9-Input OR Gate with Non-Inverted Inputs
SOP3	Macro: Sum of Products
SOP3B1A	Macro: Sum of Products
SOP3B1B	Macro: Sum of Products
SOP3B2A	Macro: Sum of Products
SOP3B2B	Macro: Sum of Products
SOP3B3	Macro: Sum of Products
SOP4	Macro: Sum of Products
SOP4B1	Macro: Sum of Products
SOP4B2A	Macro: Sum of Products
SOP4B2B	Macro: Sum of Products
SOP4B3	Macro: Sum of Products
SOP4B4	Macro: Sum of Products
XNOR2	Primitive: 2-Input XNOR Gate with Non-Inverted Inputs
XNOR3	Primitive: 3-Input XNOR Gate with Non-Inverted Inputs
XNOR4	Primitive: 4-Input XNOR Gate with Non-Inverted Inputs
XNOR5	Primitive: 5-Input XNOR Gate with Non-Inverted Inputs
XNOR6	Macro: 6-Input XNOR Gate with Non-Inverted Inputs
XNOR7	Macro: 7-Input XNOR Gate with Non-Inverted Inputs
XNOR8	Macro: 8-Input XNOR Gate with Non-Inverted Inputs
XNOR9	Macro: 9-Input XNOR Gate with Non-Inverted Inputs
XOR2	Primitive: 2-Input XOR Gate with Non-Inverted Inputs
XOR3	Primitive: 3-Input XOR Gate with Non-Inverted Inputs
XOR4	Primitive: 4-Input XOR Gate with Non-Inverted Inputs
XOR5	Primitive: 5-Input XOR Gate with Non-Inverted Inputs
XOR6	Macro: 6-Input XOR Gate with Non-Inverted Inputs
XOR7	Macro: 7-Input XOR Gate with Non-Inverted Inputs
XOR8	Macro: 8-Input XOR Gate with Non-Inverted Inputs
XOR9	Macro: 9-Input XOR Gate with Non-Inverted Inputs

LUT

Design Element	Description
LUT1	Primitive: 1-Bit Look-Up-Table with General Output
LUT1_D	Primitive: 1-Bit Look-Up-Table with Dual Output
LUT1_L	Primitive: 1-Bit Look-Up-Table with Local Output
LUT2	Primitive: 2-Bit Look-Up-Table with General Output
LUT2_D	Primitive: 2-Bit Look-Up-Table with Dual Output
LUT2_L	Primitive: 2-Bit Look-Up-Table with Local Output
LUT3	Primitive: 3-Bit Look-Up-Table with General Output
LUT3_D	Primitive: 3-Bit Look-Up-Table with Dual Output
LUT3_L	Primitive: 3-Bit Look-Up-Table with Local Output
LUT4	Primitive: 4-Bit Look-Up-Table with General Output
LUT4_D	Primitive: 4-Bit Look-Up-Table with Dual Output
LUT4_L	Primitive: 4-Bit Look-Up-Table with Local Output

Memory

Design Element	Description
RAM16X1D	Primitive: 16-Deep by 1-Wide Static Dual Port Synchronous RAM
RAM16X1S	Primitive: 16-Deep by 1-Wide Static Synchronous RAM
RAM32X1S	Primitive: 32-Deep by 1-Wide Static Synchronous RAM
RAM64X1S	Primitive: 64-Deep by 1-Wide Static Synchronous RAM
RAMB16BWE	Primitive: 16K-bit Data and 2K-bit Parity Configurable Synchronous Dual Port Block RAM
RAMB16BWE_S18	Primitive: 16K-bit Data and 2K-bit Parity Synchronous Single Port Block RAM with 18-bit Port
RAMB16BWE_S18_S18	Primitive: 16K-bit Data and 2K-bit Parity Synchronous Dual Port Block RAM with 18-bit Ports
RAMB16BWE_S18_S9	Primitive: 16K-bit Data and 2K-bit Parity Synchronous Dual Port Block RAM with 18-bit and 9-bit Ports
RAMB16BWE_S36	Primitive: 16K-bit Data and 2K-bit Parity Synchronous Single Port Block RAM with 36-Bit Port
RAMB16BWE_S36_S18	Primitive: 16K-bit Data and 2K-bit Parity Synchronous Dual Port Block RAM with 36-bit and 18-bit Ports
RAMB16BWE_S36_S36	Primitive: 16K-bit Data and 2K-bit Parity Synchronous Dual Port Block RAM with 36-bit Ports
RAMB16BWE_S36_S9	Primitive: 16K-bit Data and 2K-bit Parity Synchronous Dual Port Block RAM with 36-bit and 9-bit Ports
RAMB16BWER	Primitive: 16K-bit Data and 2K-bit Parity Configurable Synchronous Dual Port Block RAM with Optional Output Registers
ROM128X1	Primitive: 128-Deep by 1-Wide ROM
ROM16X1	Primitive: 16-Deep by 1-Wide ROM
ROM256X1	Primitive: 256-Deep by 1-Wide ROM

Design Element	Description
ROM32X1	Primitive: 32-Deep by 1-Wide ROM
ROM64X1	Primitive: 64-Deep by 1-Wide ROM

Mux

Design Element	Description
M16_1E	Macro: 16-to-1 Multiplexer with Enable
M2_1	Macro: 2-to-1 Multiplexer
M2_1B1	Macro: 2-to-1 Multiplexer with D0 Inverted
M2_1B2	Macro: 2-to-1 Multiplexer with D0 and D1 Inverted
M2_1E	Macro: 2-to-1 Multiplexer with Enable
M4_1E	Macro: 4-to-1 Multiplexer with Enable
M8_1E	Macro: 8-to-1 Multiplexer with Enable
MUXF5	Primitive: 2-to-1 Look-Up Table Multiplexer with General Output
MUXF5_D	Primitive: 2-to-1 Look-Up Table Multiplexer with Dual Output
MUXF5_L	Primitive: 2-to-1 Look-Up Table Multiplexer with Local Output
MUXF6	Primitive: 2-to-1 Look-Up Table Multiplexer with General Output
MUXF6_D	Primitive: 2-to-1 Look-Up Table Multiplexer with Dual Output
MUXF6_L	Primitive: 2-to-1 Look-Up Table Multiplexer with Local Output
MUXF7	Primitive: 2-to-1 Look-Up Table Multiplexer with General Output
MUXF7_D	Primitive: 2-to-1 Look-Up Table Multiplexer with Dual Output
MUXF7_L	Primitive: 2-to-1 Look-Up Table Multiplexer with Local Output
MUXF8	Primitive: 2-to-1 Look-Up Table Multiplexer with General Output
MUXF8_D	Primitive: 2-to-1 Look-Up Table Multiplexer with Dual Output
MUXF8_L	Primitive: 2-to-1 Look-Up Table Multiplexer with Local Output

Shift Register

Design Element	Description
SR16CE	Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR16CLE	Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR16CLED	Macro: 16-Bit Shift Register with Clock Enable and Asynchronous Clear
SR16RE	Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR16RLE	Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR16RLED	Macro: 16-Bit Shift Register with Clock Enable and Synchronous Reset

Design Element	Description
SR4CE	Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR4CLE	Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR4CLED	Macro: 4-Bit Shift Register with Clock Enable and Asynchronous Clear
SR4RE	Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR4RLE	Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR4RLED	Macro: 4-Bit Shift Register with Clock Enable and Synchronous Reset
SR8CE	Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR8CLE	Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear
SR8CLED	Macro: 8-Bit Shift Register with Clock Enable and Asynchronous Clear
SR8RE	Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR8RLE	Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset
SR8RLED	Macro: 8-Bit Shift Register with Clock Enable and Synchronous Reset
SRL16	Primitive: 16-Bit Shift Register Look-Up-Table (LUT)
SRL16_1	Primitive: 16-Bit Shift Register Look-Up-Table (LUT) with Negative-Edge Clock
SRL16E	Primitive: 16-Bit Shift Register Look-Up-Table (LUT) with Clock Enable
SRL16E_1	Primitive: 16-Bit Shift Register Look-Up-Table (LUT) with Negative-Edge Clock and Clock Enable
SRLC16	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry
SRLC16_1	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry and Negative-Edge Clock
SRLC16E	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry and Clock Enable
SRLC16E_1	Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry, Negative-Edge Clock, and Clock Enable

Shifter

Design Element	Description
BRLSHFT4	Macro: 4-Bit Barrel Shifter
BRLSHFT8	Macro: 8-Bit Barrel Shifter

About Design Elements

This section describes the design elements that can be used with this architecture. The design elements are organized alphabetically.

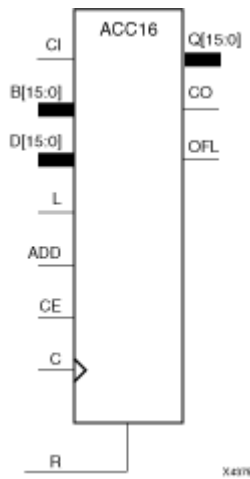
The following information is provided for each design element, where applicable:

- Name of element
- Brief description
- Schematic symbol (if any)
- Logic Table (if any)
- Port Descriptions (if any)
- Usage
- Available Attributes (if any)
- For more information

You can find examples of VHDL and Verilog instantiation code in the ISE software (in the main menu, select **Edit** > **Language Templates** or in the *Libraries Guide for HDL Designs* for this architecture.

ACC16

Macro: 16-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset



Introduction

This design element can add or subtract a 16-bit unsigned-binary, respectively or twos-complement word to or from the contents of a 16-bit data register and store the results in the register. The register can be loaded with the 16-bit word.

When the load input (L) is High, CE is ignored and the data on the D inputs is loaded into the register during the Low-to-High clock (C) transition. ACC16 loads the data on inputs D15 – D0 into the 16-bit register.

This design element operates on either 16-bit unsigned binary numbers or 16-bit twos-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as twos complement, the output can be interpreted as twos complement. The only functional difference between an unsigned binary operation and a twos-complement operation is how they determine when “overflow” occurs. Unsigned binary uses carry-out (CO), while twos complement uses OFL to determine when “overflow” occurs.

- For unsigned binary operation, ACC16 can represent numbers between 0 and 15, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtractor. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds. The carry-out (CO) is not registered synchronously with the data outputs. CO always reflects the accumulation of the B inputs (B15 – B0 for ACC16). This allows the cascading of ACC16s by connecting CO of one stage to CI of the next stage. An unsigned binary “overflow” that is always active-High can be generated by gating the ADD signal and CO as follows:

$\text{unsigned overflow} = \text{CO XOR ADD}$

Ignore OFL in unsigned binary operation.

- For twos-complement operation, ACC16 represents numbers between -8 and +7, inclusive. If an addition or subtraction operation result exceeds this range, the OFL output goes High. The overflow (OFL) is not registered synchronously with the data outputs. OFL always reflects the accumulation of the B inputs (B15 – B0 for ACC16) and the contents of the register, which allows cascading of ACC4s by connecting OFL of one stage to CI of the next stage.

Ignore CO in twos-complement operation.

The synchronous reset (R) has priority over all other inputs, and when set to High, causes all outputs to go to logic level zero during the Low-to-High clock (C) transition. Clock (C) transitions are ignored when clock enable (CE) is Low.

This design element is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Input						Output
R	L	CE	ADD	D	C	Q
1	x	x	x	x	Rising	0
0	1	x	x	Dn	Rising	Dn
0	0	1	1	x	Rising	Q0+Bn+CI
0	0	1	0	x	Rising	Q0-Bn-CI
0	0	0	x	x	Rising	No Change

Q0: Previous value of Q
 Bn: Value of Data input B
 CI: Value of input CI

Design Entry Method

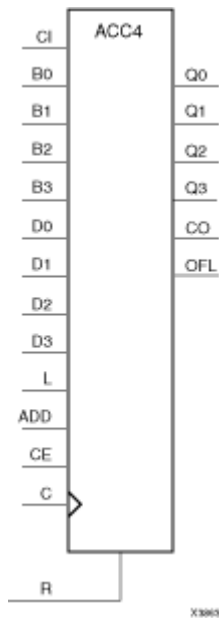
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ACC4

Macro: 4-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset



Introduction

This design element can add or subtract a 4-bit unsigned-binary, respectively or twos-complement word to or from the contents of a 4-bit data register and store the results in the register. The register can be loaded with the 4-bit word.

When the load input (L) is High, CE is ignored and the data on the D inputs is loaded into the register during the Low-to-High clock (C) transition. ACC4 loads the data on inputs D3 – D0 into the 4-bit register.

This design element operates on either 4-bit unsigned binary numbers or 4-bit twos-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as twos complement, the output can be interpreted as twos complement. The only functional difference between an unsigned binary operation and a twos-complement operation is how they determine when “overflow” occurs. Unsigned binary uses carry-out (CO), while twos complement uses OFL to determine when “overflow” occurs.

- For unsigned binary operation, ACC4 can represent numbers between 0 and 15, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtractor. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds. The carry-out (CO) is not registered synchronously with the data outputs. CO always reflects the accumulation of the B inputs (B3 – B0 for ACC4). This allows the cascading of ACC4s by connecting CO of one stage to CI of the next stage. An unsigned binary “overflow” that is always active-High can be generated by gating the ADD signal and CO as follows:

unsigned overflow = CO XOR ADD

Ignore OFL in unsigned binary operation.

- For twos-complement operation, ACC4 represents numbers between -8 and +7, inclusive. If an addition or subtraction operation result exceeds this range, the OFL output goes High. The overflow (OFL) is not registered synchronously with the data outputs. OFL always reflects the accumulation of the B inputs (B3 – B0 for ACC4) and the contents of the register, which allows cascading of ACC4s by connecting OFL of one stage to CI of the next stage.

Ignore CO in twos-complement operation.

The synchronous reset (R) has priority over all other inputs, and when set to High, causes all outputs to go to logic level zero during the Low-to-High clock (C) transition. Clock (C) transitions are ignored when clock enable (CE) is Low.

This design element is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Input						Output
R	L	CE	ADD	D	C	Q
1	x	x	x	x	Rising	0
0	1	x	x	Dn	Rising	Dn
0	0	1	1	x	Rising	Q0+Bn+CI
0	0	1	0	x	Rising	Q0-Bn-CI
0	0	0	x	x	Rising	No Change

Q0: Previous value of Q
 Bn: Value of Data input B
 CI: Value of input CI

Design Entry Method

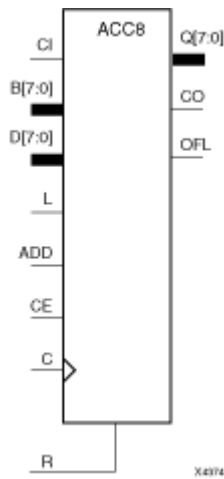
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ACC8

Macro: 8-Bit Loadable Cascadable Accumulator with Carry-In, Carry-Out, and Synchronous Reset



Introduction

This design element can add or subtract a 8-bit unsigned-binary, respectively or twos-complement word to or from the contents of a 8-bit data register and store the results in the register. The register can be loaded with the 8-bit word.

When the load input (L) is High, CE is ignored and the data on the D inputs is loaded into the register during the Low-to-High clock (C) transition. ACC8 loads the data on inputs D7 – D0 into the 8-bit register.

This design element operates on either 8-bit unsigned binary numbers or 8-bit twos-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as twos complement, the output can be interpreted as twos complement. The only functional difference between an unsigned binary operation and a twos-complement operation is how they determine when “overflow” occurs. Unsigned binary uses carry-out (CO), while twos complement uses OFL to determine when “overflow” occurs.

- For unsigned binary operation, ACC8 can represent numbers between 0 and 255, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtractor. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds. The carry-out (CO) is not registered synchronously with the data outputs. CO always reflects the accumulation of the B inputs (B3 – B0 for ACC4). This allows the cascading of ACC8s by connecting CO of one stage to CI of the next stage. An unsigned binary “overflow” that is always active-High can be generated by gating the ADD signal and CO as follows:

unsigned overflow = CO XOR ADD

Ignore OFL in unsigned binary operation.

- For twos-complement operation, ACC8 represents numbers between -128 and +127, inclusive. If an addition or subtraction operation result exceeds this range, the OFL output goes High. The overflow (OFL) is not registered synchronously with the data outputs. OFL always reflects the accumulation of the B inputs (B3 – B0 for ACC8) and the contents of the register, which allows cascading of ACC8s by connecting OFL of one stage to CI of the next stage.

Ignore CO in twos-complement operation.

The synchronous reset (R) has priority over all other inputs, and when set to High, causes all outputs to go to logic level zero during the Low-to-High clock (C) transition. Clock (C) transitions are ignored when clock enable (CE) is Low.

This design element is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Input						Output
R	L	CE	ADD	D	C	Q
1	x	x	x	x	Rising	0
0	1	x	x	Dn	Rising	Dn
0	0	1	1	x	Rising	Q0+Bn+CI
0	0	1	0	x	Rising	Q0-Bn-CI
0	0	0	x	x	Rising	No Change

Q0: Previous value of Q
 Bn: Value of Data input B
 CI: Value of input CI

Design Entry Method

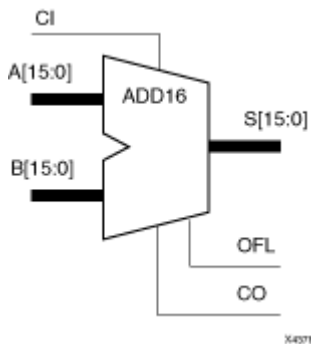
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ADD16

Macro: 16-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow



Introduction

This design element adds two words and a carry-in (CI), producing a sum output and carry-out (CO) or overflow (OFL). The factors added are $A_{15} - A_0$, $B_{15} - B_0$ and CI, producing the sum output $S_{15} - S_0$ and CO (or OFL).

Logic Table

Input		Output
A	B	S
A_n	B_n	$A_n + B_n + CI$
CI: Value of input CI.		

Unsigned Binary Versus Twos Complement

This design element can operate on either 16-bit unsigned binary numbers or 16-bit twos-complement numbers, respectively. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as twos complement, the output can be interpreted as twos complement. The only functional difference between an unsigned binary operation and a twos-complement operation is the way they determine when “overflow” occurs. Unsigned binary uses CO, while twos-complement uses OFL to determine when “overflow” occurs. To interpret the inputs as unsigned binary, follow the CO output. To interpret the inputs as twos complement, follow the OFL output.

Unsigned Binary Operation

For unsigned binary operation, this element represents numbers between 0 and 65535, inclusive. OFL is ignored in unsigned binary operation.

Twos-Complement Operation

For twos-complement operation, this element can represent numbers between -32768 and +32767, inclusive. OFL is active (High) when the sum exceeds the bounds of the adder. CO is ignored in twos-complement operation.

Design Entry Method

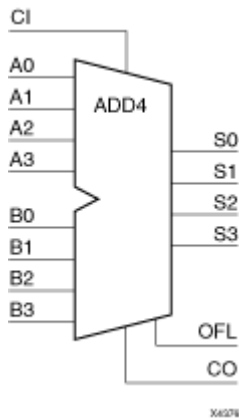
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ADD4

Macro: 4-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow



Introduction

This design element adds two words and a carry-in (CI), producing a sum output and carry-out (CO) or overflow (OFL). The factors added are A3 – A0, B3 – B0, and CI producing the sum output S3 – S0 and CO (or OFL).

Logic Table

Input		Output
A	B	S
A _n	B _n	A _n +B _n +CI
CI: Value of input CI.		

Unsigned Binary Versus Twos Complement

This design element can operate on either 4-bit unsigned binary numbers or 4-bit twos-complement numbers, respectively. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as twos complement, the output can be interpreted as twos complement. The only functional difference between an unsigned binary operation and a twos-complement operation is the way they determine when “overflow” occurs. Unsigned binary uses CO, while twos-complement uses OFL to determine when “overflow” occurs. To interpret the inputs as unsigned binary, follow the CO output. To interpret the inputs as twos complement, follow the OFL output.

Unsigned Binary Operation

For unsigned binary operation, this element represents numbers from 0 to 15, inclusive. OFL is ignored in unsigned binary operation.

Twos-Complement Operation

For twos-complement operation, this element can represent numbers between -8 and +7, inclusive. OFL is active (High) when the sum exceeds the bounds of the adder. CO is ignored in twos-complement operation.

Design Entry Method

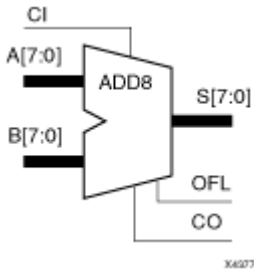
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ADD8

Macro: 8-Bit Cascadable Full Adder with Carry-In, Carry-Out, and Overflow



Introduction

This design element adds two words and a carry-in (CI), producing a sum output and carry-out (CO) or overflow (OFL). The factors added are $A_7 - A_0$, $B_7 - B_0$, and CI, producing the sum output $S_7 - S_0$ and CO (or OFL).

Logic Table

Input		Output
A	B	S
A_n	B_n	$A_n + B_n + CI$
CI: Value of input CI.		

Unsigned Binary Versus Twos Complement

This design element can operate on either 8-bit unsigned binary numbers or 8-bit twos-complement numbers, respectively. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as twos complement, the output can be interpreted as twos complement. The only functional difference between an unsigned binary operation and a twos-complement operation is the way they determine when “overflow” occurs. Unsigned binary uses CO, while twos-complement uses OFL to determine when “overflow” occurs. To interpret the inputs as unsigned binary, follow the CO output. To interpret the inputs as twos complement, follow the OFL output.

Unsigned Binary Operation

For unsigned binary operation, this element represents numbers between 0 and 255, inclusive. OFL is ignored in unsigned binary operation.

Twos-Complement Operation

For twos-complement operation, this element can represent numbers between -128 and +127, inclusive. OFL is active (High) when the sum exceeds the bounds of the adder. CO is ignored in twos-complement operation.

Design Entry Method

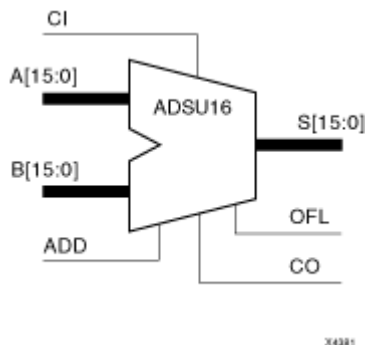
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ADSU16

Macro: 16-Bit Cascadable Adder/Subtractor with Carry-In, Carry-Out, and Overflow



Introduction

When the ADD input is High, ADSU16 adds two 16-bit words ($A_{15} - A_0$ and $B_{15} - B_0$) and a CI are added, producing a 16-bit sum output ($S_{15} - S_0$) and CO or OFL. ADSU4 adds two 4-bit words ($A_3 - A_0$ and $B_3 - B_0$) and a CI, producing a 4-bit sum output ($S_3 - S_0$) and CO or OFL. ADSU8 adds two 8-bit words ($A_7 - A_0$ and $B_7 - B_0$) and a CI producing, an 8-bit sum output ($S_7 - S_0$) and CO or OFL. ADSU16 adds two 16-bit words ($A_{15} - A_0$ and $B_{15} - B_0$) and a CI, producing a 16-bit sum output ($S_{15} - S_0$) and CO or OFL.

When the ADD input is Low, this element subtracts $B_z - B_0$ from $A_z - A_0$, producing a difference output and CO or OFL. It subtracts $B_3 - B_0$ from $A_3 - A_0$, producing a 4-bit difference ($S_3 - S_0$) and CO or OFL.

In add mode, CO and CI are active-High. In subtract mode, CO and CI are active-Low. OFL is active-High in add and subtract modes.

Logic Table

Input			Output
ADD	A	B	S
1	A_n	B_n	$A_n + B_n + CI^*$
0	A_n	B_n	$A_n - B_n - CI^*$
CI*: ADD = 0, CI, CO active LOW			
CI*: ADD = 1, CI, CO active HIGH			

Unsigned Binary Versus Twos Complement

This design element can operate on either 16-bit unsigned binary numbers or 16-bit twos-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as twos complement, the output can be interpreted as twos complement. The only functional difference between an unsigned binary operation and a twos-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while twos complement uses OFL to determine when "overflow" occurs.

With adder/subtractors, either unsigned binary or twos-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated.

Unsigned Binary Operation

For unsigned binary operation, this element can represent numbers between 0 and 65535, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtractor. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds.

An unsigned binary “overflow” that is always active-High can be generated by gating the ADD signal and CO as follows:

$\text{unsigned overflow} = \text{CO XOR ADD}$

OFL is ignored in unsigned binary operation.

Twos-Complement Operation

For twos-complement operation, this element can represent numbers between -32768 and +32767, inclusive.

If an addition or subtraction operation result exceeds this range, the OFL output goes High. CO is ignored in twos-complement operation.

Design Entry Method

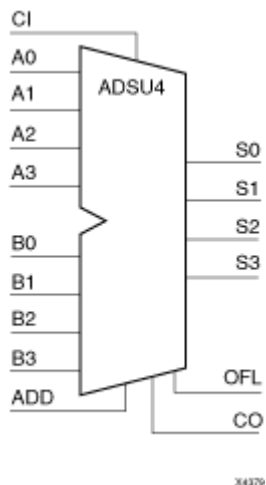
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ADSU4

Macro: 4-Bit Cascadable Adder/Subtractor with Carry-In, Carry-Out, and Overflow



Introduction

When the ADD input is High, ADSU4 adds two 4-bit words ($A_3 - A_0$ and $B_3 - B_0$) and a CI are added, producing a 4-bit sum output ($S_3 - S_0$) and CO or OFL. For this element, two 4-bit words ($A_3 - A_0$ and $B_3 - B_0$) and a CI are added, producing a 4-bit sum output ($S_3 - S_0$) and CO or OFL.

When the ADD input is Low, this element subtracts $B_3 - B_0$ from $A_3 - A_0$, producing a 4-bit difference ($S_3 - S_0$) and CO or OFL.

In add mode, CO and CI are active-High. In subtract mode, CO and CI are active-Low. OFL is active-High in add and subtract modes.

Logic Table

Input			Output
ADD	A	B	S
1	A_n	B_n	$A_n + B_n + CI^*$
0	A_n	B_n	$A_n - B_n - CI^*$
CI*: ADD = 0, CI, CO active LOW			
CI*: ADD = 1, CI, CO active HIGH			

Unsigned Binary Versus Twos Complement

This design element can operate on either 4-bit unsigned binary numbers or 4-bit twos-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as twos complement, the output can be interpreted as twos complement. The only functional difference between an unsigned binary operation and a twos-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while twos complement uses OFL to determine when "overflow" occurs.

With adder/subtractors, either unsigned binary or twos-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated.

Unsigned Binary Operation

For unsigned binary operation, ADSU4 can represent numbers between 0 and 15, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtractor. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds.

An unsigned binary “overflow” that is always active-High can be generated by gating the ADD signal and CO as follows:

$$\text{unsigned overflow} = \text{CO XOR ADD}$$

OFL is ignored in unsigned binary operation.

Twos-Complement Operation

For twos-complement operation, this element can represent numbers between -8 and +7, inclusive.

If an addition or subtraction operation result exceeds this range, the OFL output goes High. CO is ignored in twos-complement operation.

Design Entry Method

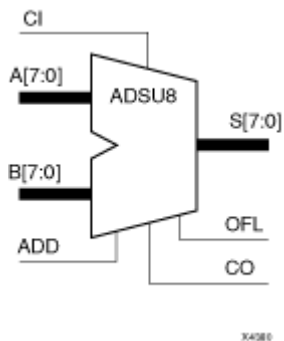
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ADSU8

Macro: 8-Bit Cascadable Adder/Subtractor with Carry-In, Carry-Out, and Overflow



Introduction

When the ADD input is High, ADSU8 adds two 8-bit words ($A_7 - A_0$ and $B_7 - B_0$) and a CI are added, producing an 8-bit sum output ($S_7 - S_0$) and CO or OFL. For this element, two 8-bit words ($A_7 - A_0$ and $B_7 - B_0$) and a CI producing, an 8-bit sum output ($S_7 - S_0$) and CO or OFL.

When the ADD input is Low, this element subtracts $B_7 - B_0$ from $A_7 - A_0$, producing an 8-bit difference ($S_7 - S_0$) and CO or OFL.

In add mode, CO and CI are active-High. In subtract mode, CO and CI are active-Low. OFL is active-High in add and subtract modes.

Logic Table

Input			Output
ADD	A	B	S
1	A_n	B_n	$A_n + B_n + CI^*$
0	A_n	B_n	$A_n - B_n - CI^*$
CI*: ADD = 0, CI, CO active LOW			
CI*: ADD = 1, CI, CO active HIGH			

Unsigned Binary Versus Twos Complement

This design element can operate on either 8-bit unsigned binary numbers or 8-bit twos-complement numbers. If the inputs are interpreted as unsigned binary, the result can be interpreted as unsigned binary. If the inputs are interpreted as twos complement, the output can be interpreted as twos complement. The only functional difference between an unsigned binary operation and a twos-complement operation is the way they determine when "overflow" occurs. Unsigned binary uses CO, while twos complement uses OFL to determine when "overflow" occurs.

With adder/subtractors, either unsigned binary or twos-complement operations cause an overflow. If the result crosses the overflow boundary, an overflow is generated. Similarly, when the result crosses the carry-out boundary, a carry-out is generated.

Unsigned Binary Operation

For unsigned binary operation, this element can represent numbers between 0 and 255, inclusive. In add mode, CO is active (High) when the sum exceeds the bounds of the adder/subtractor. In subtract mode, CO is an active-Low borrow-out and goes Low when the difference exceeds the bounds.

An unsigned binary "overflow" that is always active-High can be generated by gating the ADD signal and CO as follows:

$$\text{unsigned overflow} = \text{CO XOR ADD}$$

OFL is ignored in unsigned binary operation.

Twos-Complement Operation

For twos-complement operation, this element can represent numbers between -128 and +127, inclusive.

If an addition or subtraction operation result exceeds this range, the OFL output goes High. CO is ignored in twos-complement operation.

Design Entry Method

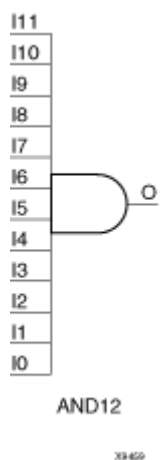
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND12

Macro: 12- Input AND Gate with Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

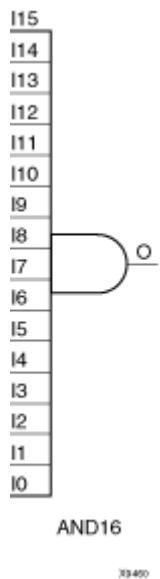
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND16

Macro: 16- Input AND Gate with Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

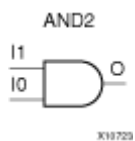
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND2

Primitive: 2-Input AND Gate with Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND2B1

Primitive: 2-Input AND Gate with 1 Inverted and 1 Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

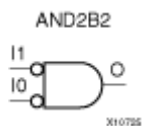
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND2B2

Primitive: 2-Input AND Gate with Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND3

Primitive: 3-Input AND Gate with Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

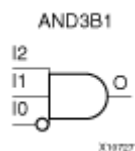
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND3B1

Primitive: 3-Input AND Gate with 1 Inverted and 2 Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

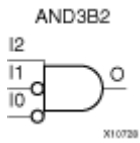
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND3B2

Primitive: 3-Input AND Gate with 2 Inverted and 1 Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

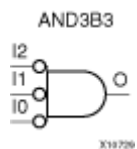
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND3B3

Primitive: 3-Input AND Gate with Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

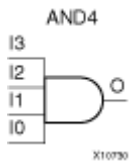
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND4

Primitive: 4-Input AND Gate with Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

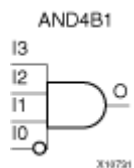
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND4B1

Primitive: 4-Input AND Gate with 1 Inverted and 3 Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

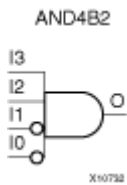
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND4B2

Primitive: 4-Input AND Gate with 2 Inverted and 2 Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

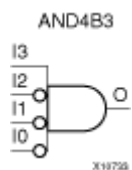
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND4B3

Primitive: 4-Input AND Gate with 3 Inverted and 1 Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

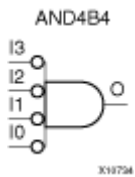
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND4B4

Primitive: 4-Input AND Gate with Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

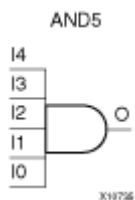
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND5

Primitive: 5-Input AND Gate with Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

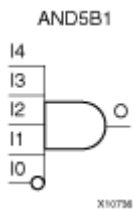
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND5B1

Primitive: 5-Input AND Gate with 1 Inverted and 4 Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

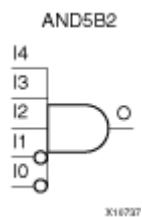
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND5B2

Primitive: 5-Input AND Gate with 2 Inverted and 3 Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

This design element is only for use in schematics.

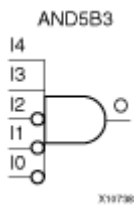
Available Attributes

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND5B3

Primitive: 5-Input AND Gate with 3 Inverted and 2 Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

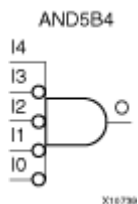
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND5B4

Primitive: 5-Input AND Gate with 4 Inverted and 1 Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

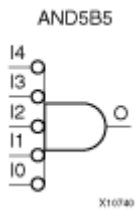
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND5B5

Primitive: 5-Input AND Gate with Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

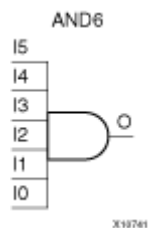
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND6

Macro: 6-Input AND Gate with Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

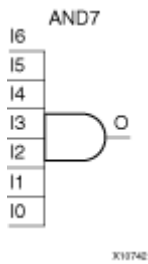
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND7

Macro: 7-Input AND Gate with Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

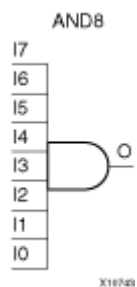
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND8

Macro: 8-Input AND Gate with Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

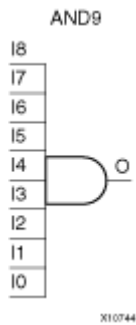
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

AND9

Macro: 9-Input AND Gate with Non-Inverted Inputs



Introduction

AND functions of up to five inputs are available in any combination of inverting and non-inverting inputs. AND functions of six to nine inputs, 12 inputs, and 16 inputs are available with noninverting inputs. To make some or all inputs inverting, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the appropriate number of inputs.

Design Entry Method

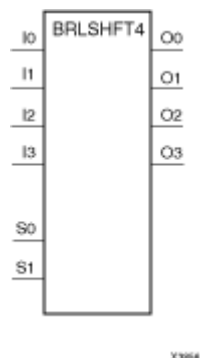
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

BRLSHFT4

Macro: 4-Bit Barrel Shifter



Introduction

This design element is a 4-bit barrel shifter that can rotate four inputs (I3 – I0) up to four places. The control inputs (S1 and S0) determine the number of positions, from one to four, that the data is rotated. The four outputs (O3 – O0) reflect the shifted data inputs.

Logic Table

Inputs						Outputs			
S1	S0	I0	I1	I2	I3	O0	O1	O2	O3
0	0	a	b	c	d	a	b	c	d
0	1	a	b	c	d	b	c	d	a
1	0	a	b	c	d	c	d	a	b
1	1	a	b	c	d	d	a	b	c

Design Entry Method

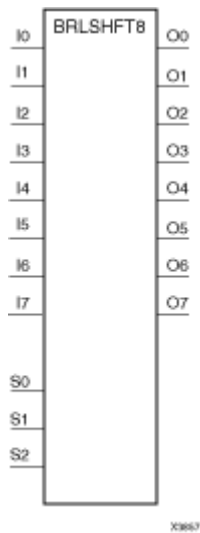
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

BRLSHFT8

Macro: 8-Bit Barrel Shifter



Introduction

This design element is an 8-bit barrel shifter, can rotate the eight inputs (I7 – I0) up to eight places. The control inputs (S2 – S0) determine the number of positions, from one to eight, that the data is rotated. The eight outputs (O7 – O0) reflect the shifted data inputs.

Logic Table

Inputs											Outputs							
S2	S1	S0	I0	I1	I2	I3	I4	I5	I6	I7	O0	O1	O2	O3	O4	O5	O6	O7
0	0	0	a	b	c	d	e	f	g	h	a	b	c	d	e	f	g	h
0	0	1	a	b	c	d	e	f	g	h	b	c	d	e	f	g	h	a
0	1	0	a	b	c	d	e	f	g	h	c	d	e	f	g	h	a	b
0	1	1	a	b	c	d	e	f	g	h	d	e	f	g	h	a	b	c
1	0	0	a	b	c	d	e	f	g	h	e	f	g	h	a	b	c	d
1	0	1	a	b	c	d	e	f	g	h	f	g	h	a	b	c	d	e
1	1	0	a	b	c	d	e	f	g	h	g	h	a	b	c	d	e	f
1	1	1	a	b	c	d	e	f	g	h	h	a	b	c	d	e	f	g

Design Entry Method

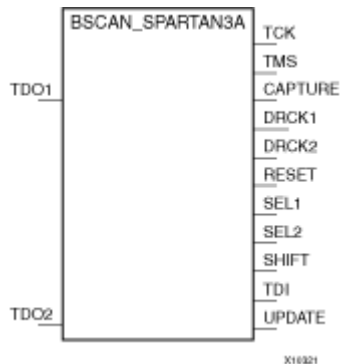
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

BSCAN_SPARTAN3A

Primitive: Spartan-3A Global Set/Reset, Global 3-State and Configuration Start-Up Clock Interface



Introduction

This design element allows access to and from the JTAG Boundary Scan logic controller from internal logic, thus accommodating communications between the internal running design and the dedicated JTAG pins of the FPGA.

Note For specific information on boundary scan for an architecture, see *The Programmable Logic Data Sheets*

Port Descriptions

Name	Direction	Width	Function
TDI	Output	1	A mirror of the TDI input pin to the FPGA.
DRCK1, DRK2	Output	1	A mirror of the TCK input pin to the FPGA when the JTAG USER instruction is loaded and the JTAG TAP controller is in the SHIFT-DR state. DRK1 applies to the USER1 logic while DRK2 applies to USER2.
RESET	Output	1	Active upon the loading of the USER instruction. It asserts High when the JTAG TAP controller is in the TEST-LOGIC-RESET state.
SEL1, SEL2	Output	1	Indicates when the USER1 or USER2 instruction has been loaded into the JTAG Instruction Register. SEL1 or SEL2 becomes active in the UPDATE-IR state, and stays active until a new instruction is loaded.
SHIFT	Output	1	Active upon the loading of the USER instruction. It asserts High when the JTAG TAP controller is in the SHIFT-DR state.
CAPTURE	Output	1	Active upon the loading of the USER instruction. Asserts High when the JTAG TAP controller is in the CAPTURE-DR state.
UPDATE	Output	1	Active upon the loading of the USER instruction. It asserts High when the JTAG TAP controller is in the UPDATE-DR state.
TDO1, TDO2	Input	1	Active upon the loading of the USER1 or USER2 instruction. External JTAG TDO pin reflects data input to the component's TDO1 (USER1) or TDO2 (USER2) pin.

Design Entry Method

This design element can be used in schematics.

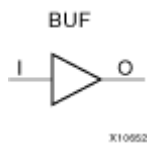
For More Information

- See the [Spartan-3A User Guide](#).

- See the [Spartan-3A Data Sheets](#).

BUF

Primitive: General Purpose Buffer



Introduction

This is a general-purpose, non-inverting buffer.

This element is not necessary and is removed by the partitioning software (MAP).

Design Entry Method

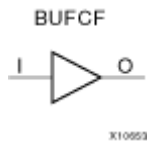
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

BUFCF

Fast Connect Buffer



Introduction

This design element is a single fast connect buffer used to connect the outputs of the LUTs and some dedicated logic directly to the input of another LUT. Using this buffer implies CLB packing. No more than four LUTs may be connected together as a group.

Design Entry Method

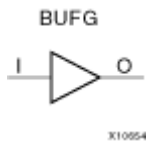
This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

BUFG

Primitive: Global Clock Buffer



Introduction

This design element is a high-fanout buffer that connects signals to the global routing resources for low skew distribution of the signal. BUFs are typically used on clock nets as well other high fanout nets like sets/resets and clock enables.

Design Entry Method

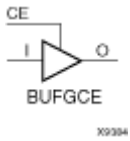
This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

BUFGCE

Primitive: Global Clock Buffer with Clock Enable



Introduction

This design element is a global clock buffer with a single gated input. Its O output is "0" when clock enable (CE) is Low (inactive). When clock enable (CE) is High, the I input is transferred to the O output.

Logic Table

Inputs		Outputs
I	CE	O
X	0	0
I	1	I

Design Entry Method

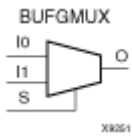
This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

BUFGMUX

Primitive: Global Clock MUX Buffer



Introduction

BUFGMUX is a multiplexed global clock buffer, based off of the BUFGCTRL, that can select between two input clocks: I0 and I1. When the select input (S) is Low, the signal on I0 is selected for output (O). When the select input (S) is High, the signal on I1 is selected for output.

BUFGMUX and BUFGMUX_1 are distinguished by the state the output assumes when that output switches between clocks in response to a change in its select input. BUFGMUX assumes output state 0 and BUFGMUX_1 assumes output state 1.

Note BUFGMUX guarantees that when S is toggled, the state of the output remains in the inactive state until the next active clock edge (either I0 or I1) occurs.

Logic Table

Inputs			Outputs
I0	I1	S	O
I0	X	0	I0
X	I1	1	I1
X	X	↑	0
X	X	↓	0

Design Entry Method

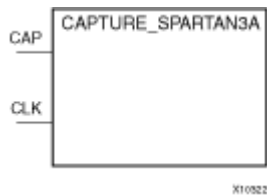
This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CAPTURE_SPARTAN3A

Primitive: Spartan-3A Register State Capture for Bitstream Readback



Introduction

This element provides user control and synchronization over when and how the capture register (flip-flop and latch) information task is requested. The readback function is provided through dedicated configuration port instructions. However, without this element, the readback data is synchronized to the configuration clock. Only register (flip-flop and latch) states can be captured. Although LUT RAM, SRL, and block RAM states are readback, they cannot be captured.

An asserted high CAP signal indicates that the registers in the device are to be captured at the next Low-to-High clock transition. By default, data is captured after every trigger when transition on CLK while CAP is asserted. To limit the readback operation to a single data capture, add the ONESHOT=TRUE attribute to this element.

Port Descriptions

Name	Direction	Width	Function
CAP	Input	1-bit	Readback capture trigger
CLK	Input	1-bit	Readback capture clock

Design Entry Method

This design element can be used in schematics.

Connect all inputs and outputs to the design in order to ensure proper operation.

Available Attributes

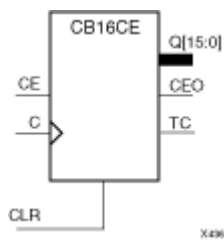
Attribute	Type	Allowed Values	Default	Description
ONESHOT	Boolean	TRUE, FALSE	TRUE	Specifies the procedure for performing single readback per CAP trigger.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CB16CE

Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs		
CLR	CE	C	Qz-Q0	TC	CEO
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO

z = bit width - 1
 $TC = Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0$
 $CEO = TC \cdot CE$

Design Entry Method

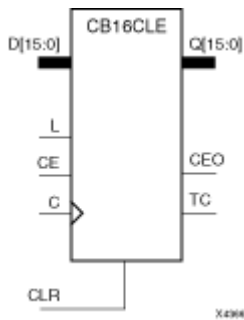
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CB16CLE

Macro: 16-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs					Outputs		
CLR	L	CE	C	Dz - D0	Qz - Q0	TC	CEO
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO

z = bit width - 1
 $TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0$
 $CEO = TC \cdot CE$

Design Entry Method

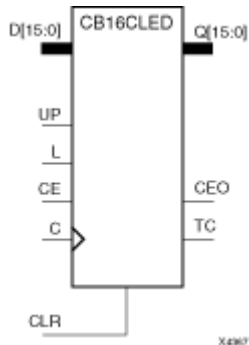
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CB16CLED

Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see "CB2X1", "CB4X1", "CB8X1", "CB16X1" for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs						Outputs		
CLR	L	CE	C	UP	Dz – D0	Qz – Q0	TC	CEO
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO

Inputs						Outputs		
CLR	L	CE	C	UP	D _z - D ₀	Q _z - Q ₀	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
z = bit width - 1 $TC = (Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0 \cdot UP) + (Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0 \cdot UP)$ $CEO = TC \cdot CE$								

Design Entry Method

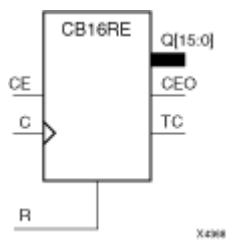
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CB16RE

Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n (t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs		
R	CE	C	Qz-Q0	TC	CEO
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
$z = \text{bit width} - 1$ $TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0$ $CEO = TC \cdot CE$					

Design Entry Method

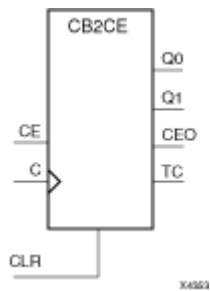
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CB2CE

Macro: 2-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs		
CLR	CE	C	Qz-Q0	TC	CEO
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO

z = bit width - 1
 $TC = Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0$
 $CEO = TC \cdot CE$

Design Entry Method

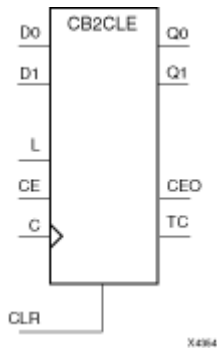
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CB2CLE

Macro: 2-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs					Outputs		
CLR	L	CE	C	D _z - D ₀	Q _z - Q ₀	TC	CEO
1	X	X	X	X	0	0	0
0	1	X	↑	D _n	D _n	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO

z = bit width - 1
 $TC = Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0$
 $CEO = TC \cdot CE$

Design Entry Method

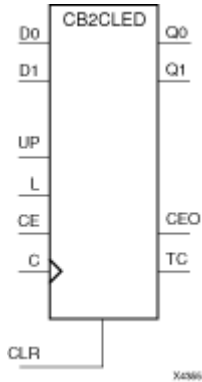
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CB2CLED

Macro: 2-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see "CB2X1", "CB4X1", "CB8X1", "CB16X1" for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs						Outputs		
CLR	L	CE	C	UP	Dz - D0	Qz - Q0	TC	CEO
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO

Inputs						Outputs		
CLR	L	CE	C	UP	D _z - D ₀	Q _z - Q ₀	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
z = bit width - 1 $TC = (Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0 \cdot UP) + (Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0 \cdot UP)$ $CEO = TC \cdot CE$								

Design Entry Method

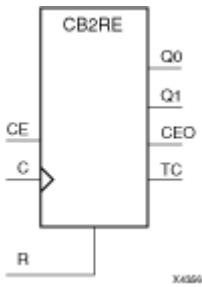
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CB2RE

Macro: 2-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs		
R	CE	C	Qz-Q0	TC	CEO
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO

z = bit width - 1
 $TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0$
 $CEO = TC \cdot CE$

Design Entry Method

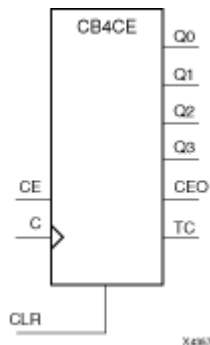
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CB4CE

Macro: 4-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs		
CLR	CE	C	Qz-Q0	TC	CEO
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO

$z = \text{bit width} - 1$
 $TC = Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0$
 $CEO = TC \cdot CE$

Design Entry Method

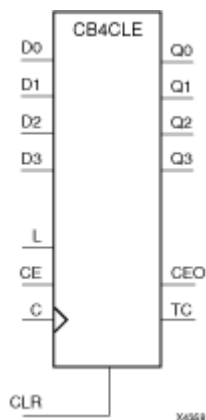
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CB4CLE

Macro: 4-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs					Outputs		
CLR	L	CE	C	D _z - D ₀	Q _z - Q ₀	TC	CEO
1	X	X	X	X	0	0	0
0	1	X	↑	D _n	D _n	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO

z = bit width - 1
 $TC = Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0$
 $CEO = TC \cdot CE$

Design Entry Method

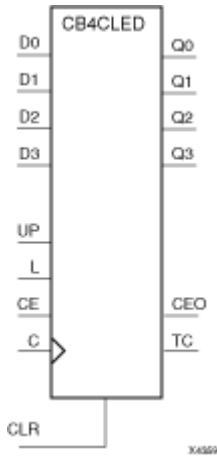
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CB4CLED

Macro: 4-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see “CB2X1”, “CB4X1”, “CB8X1”, “CB16X1” for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs						Outputs		
CLR	L	CE	C	UP	Dz – D0	Qz – Q0	TC	CEO
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO

Inputs						Outputs		
CLR	L	CE	C	UP	D _z - D ₀	Q _z - Q ₀	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
z = bit width - 1 $TC = (Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0 \cdot UP) + (Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0 \cdot UP)$ $CEO = TC \cdot CE$								

Design Entry Method

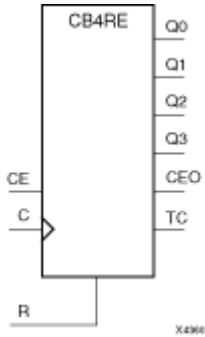
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CB4RE

Macro: 4-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs		
R	CE	C	Qz-Q0	TC	CEO
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO

$z = \text{bit width} - 1$
 $TC = Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0$
 $CEO = TC \cdot CE$

Design Entry Method

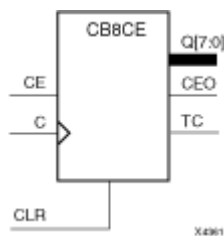
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CB8CE

Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs		
CLR	CE	C	Qz-Q0	TC	CEO
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO

z = bit width - 1
 $TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0$
 $CEO = TC \cdot CE$

Design Entry Method

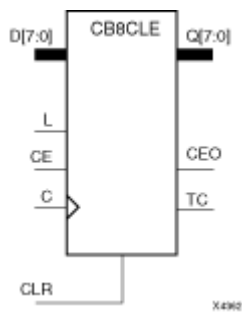
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CB8CLE

Macro: 8-Bit Loadable Cascadable Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This element is a synchronously loadable, asynchronously clearable, cascadable binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs					Outputs		
CLR	L	CE	C	D _z - D ₀	Q _z - Q ₀	TC	CEO
1	X	X	X	X	0	0	0
0	1	X	↑	D _n	D _n	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO

$z = \text{bit width} - 1$
 $TC = Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0$
 $CEO = TC \cdot CE$

Design Entry Method

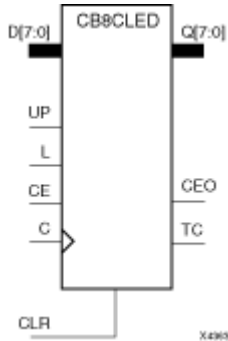
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CB8CLED

Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counters with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

For CPLD parts, see “CB2X1”, “CB4X1”, “CB8X1”, “CB16X1” for high-performance cascadable, bidirectional counters.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs						Outputs		
CLR	L	CE	C	UP	Dz - D0	Qz - Q0	TC	CEO
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO

Inputs						Outputs		
CLR	L	CE	C	UP	D _z - D ₀	Q _z - Q ₀	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO
$z = \text{bit width} - 1$ $TC = (Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0 \cdot UP) + (Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0 \cdot UP)$ $CEO = TC \cdot CE$								

Design Entry Method

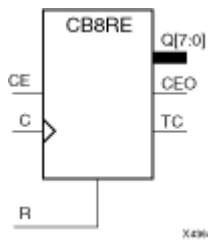
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CB8RE

Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous, resettable, cascadable binary counter. The synchronous reset (R), when High, overrides all other inputs and forces the Q outputs, terminal count (TC), and clock enable out (CEO) to zero on the Low-to-High clock transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when both Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs		
R	CE	C	Q _z -Q ₀	TC	CEO
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO
z = bit width - 1 $TC = Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0$ $CEO = TC \cdot CE$					

Design Entry Method

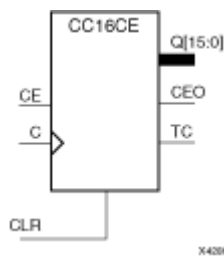
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CC16CE

Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. It is implemented using carry logic with relative location constraints to ensure efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs		
CLR	CE	C	Q _z -Q ₀	TC	CEO
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO

z = bit width - 1
 $TC = Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0$
 $CEO = TC \cdot CE$

Design Entry Method

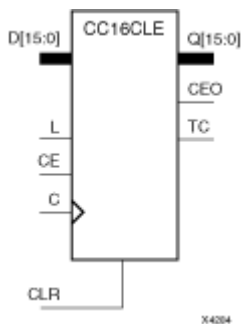
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CC16CLE

Macro: 16-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable binary counter. It is implemented using carry logic with relative location constraints to ensure efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs					Outputs		
CLR	L	CE	C	Dz - D0	Qz - Q0	TC	CEO
1	X	X	X	X	0	0	0
0	1	X	↑	Dn	Dn	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO

z = bit width - 1
 $TC = Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0$
 $CEO = TC \cdot CE$

Design Entry Method

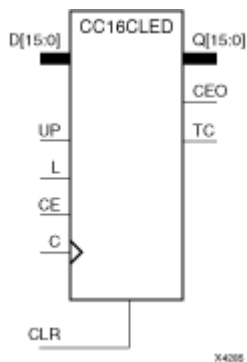
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CC16CLED

Macro: 16-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. It is implemented using carry logic with relative location constraints, which assures most efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs						Outputs		
CLR	L	CE	C	UP	Dz - D0	Qz - Q0	TC	CEO
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO

z = bit width - 1

$$TC = (Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0 \cdot UP) + (Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0 \cdot \overline{UP})$$

$$CEO = TC \cdot CE$$

Design Entry Method

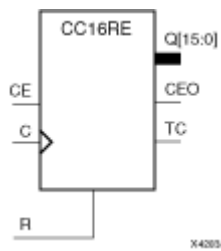
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CC16RE

Macro: 16-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous resettable, cascadable binary counter. These counters are implemented using carry logic with relative location constraints to ensure efficient logic placement. The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs and CE are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n (t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs		
R	CE	C	Q _z -Q ₀	TC	CEO
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO

$z = \text{bit width} - 1$
 $TC = Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0$
 $CEO = TC \cdot CE$

Design Entry Method

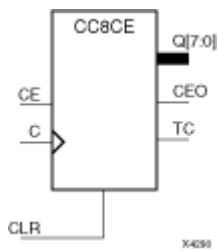
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CC8CE

Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an asynchronously clearable, cascadable binary counter. It is implemented using carry logic with relative location constraints to ensure efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs		
CLR	CE	C	Q _z -Q ₀	TC	CEO
1	X	X	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO

z = bit width - 1
 $TC = Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0$
 $CEO = TC \cdot CE$

Design Entry Method

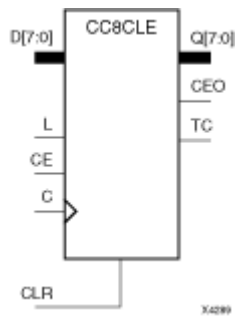
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CC8CLE

Macro: 8-Bit Loadable Cascadable Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable binary counter. It is implemented using carry logic with relative location constraints to ensure efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs increment when CE is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs					Outputs		
CLR	L	CE	C	D _z - D ₀	Q _z - Q ₀	TC	CEO
1	X	X	X	X	0	0	0
0	1	X	↑	D _n	D _n	TC	CEO
0	0	0	X	X	No change	No change	0
0	0	1	↑	X	Inc	TC	CEO

z = bit width - 1
 $TC = Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0$
 $CEO = TC \cdot CE$

Design Entry Method

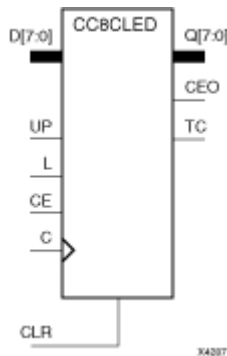
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CC8CLED

Macro: 8-Bit Loadable Cascadable Bidirectional Binary Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a synchronously loadable, asynchronously clearable, cascadable, bidirectional binary counter. It is implemented using carry logic with relative location constraints, which assures most efficient logic placement. The asynchronous clear (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition, independent of the state of clock enable (CE). The Q outputs decrement when CE is High and UP is Low during the Low-to-High clock transition. The Q outputs increment when CE and UP are High. The counter ignores clock transitions when CE is Low.

For counting up, the TC output is High when all Q outputs and UP are High. For counting down, the TC output is High when all Q outputs and UP are Low.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, UP, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs						Outputs		
CLR	L	CE	C	UP	Dz - D0	Qz - Q0	TC	CEO
1	X	X	X	X	X	0	0	0
0	1	X	↑	X	Dn	Dn	TC	CEO
0	0	0	X	X	X	No change	No change	0
0	0	1	↑	1	X	Inc	TC	CEO
0	0	1	↑	0	X	Dec	TC	CEO

$z = \text{bit width} - 1$

$$TC = (Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0 \cdot UP) + (Qz \cdot Q(z-1) \cdot Q(z-2) \cdot \dots \cdot Q0 \cdot \overline{UP})$$

$$CEO = TC \cdot CE$$

Design Entry Method

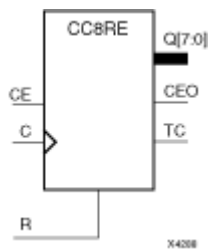
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CC8RE

Macro: 8-Bit Cascadable Binary Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a synchronous resettable, cascadable binary counter. These counters are implemented using carry logic with relative location constraints to ensure efficient logic placement. The synchronous reset (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when all Q outputs and CE are High.

Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n \cdot t_{CE-TC}$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs		
R	CE	C	Qz-Q0	TC	CEO
1	X	↑	0	0	0
0	0	X	No change	No change	0
0	1	↑	Inc	TC	CEO

z = bit width - 1
 $TC = Q_z \cdot Q_{(z-1)} \cdot Q_{(z-2)} \cdot \dots \cdot Q_0$
 $CEO = TC \cdot CE$

Design Entry Method

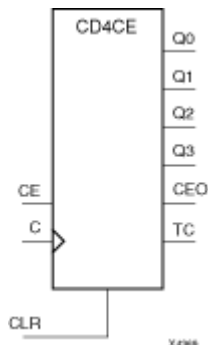
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CD4CE

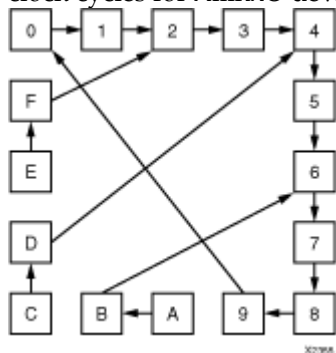
Macro: 4-Bit Cascadable BCD Counter with Clock Enable and Asynchronous Clear



Introduction

CD4CE is a 4-bit (stage), asynchronous clearable, cascadable binary-coded-decimal (BCD) counter. The asynchronous clear input (CLR) is the highest priority input. When CLR is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The Q outputs increment when clock enable (CE) is High during the Low-to-High clock (C) transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs			Outputs					
CLR	CE	C	Q3	Q2	Q1	Q0	TC	CEO
1	X	X	0	0	0	0	0	0
0	1	↑	Inc	Inc	Inc	Inc	TC	CEO

Inputs			Outputs					
CLR	CE	C	Q3	Q2	Q1	Q0	TC	CEO
0	0	X	No Change	No Change	No Change	No Change	TC	0
0	1	X	1	0	0	1	1	1
$TC = Q3 \cdot !Q2 \cdot !Q1 \cdot Q0$ $CEO = TC \cdot CE$								

Design Entry Method

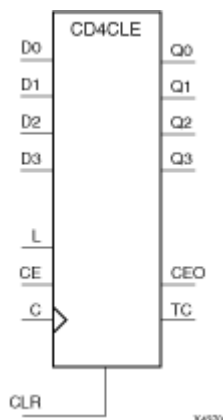
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CD4CLE

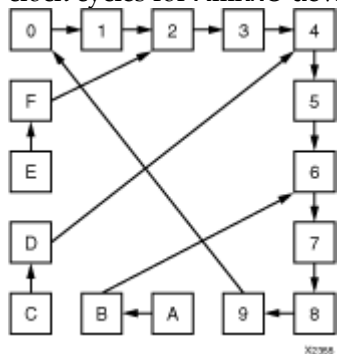
Macro: 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Asynchronous Clear



Introduction

CD4CLE is a 4-bit (stage), synchronously loadable, asynchronously clearable, binary-coded-decimal (BCD) counter. The asynchronous clear input (CLR) is the highest priority input. When (CLR) is High, all other inputs are ignored; the (Q) outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero, independent of clock transitions. The data on the (D) inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition. The (Q) outputs increment when clock enable input (CE) is High during the Low- to-High clock transition. The counter ignores clock transitions when (CE) is Low. The (TC) output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and CLR inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs					Outputs					
CLR	L	CE	D3 – D0	C	Q3	Q2	Q1	Q0	TC	CEO
1	X	X	X	X	0	0	0	0	0	0
0	1	X	D3 – D0	↑	D3	D2	D1	D0	TC	CEO
0	0	1	X	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	0	X	X	No Change	No Change	No Change	No Change	TC	0
0	0	1	X	X	1	0	0	1	1	1

$TC = Q3 \cdot !Q2 \cdot !Q1 \cdot Q0$
 $CEO = TC \cdot CE$

Design Entry Method

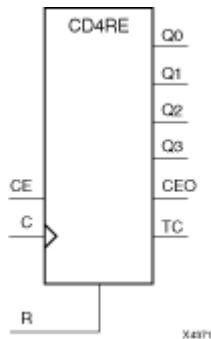
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CD4RE

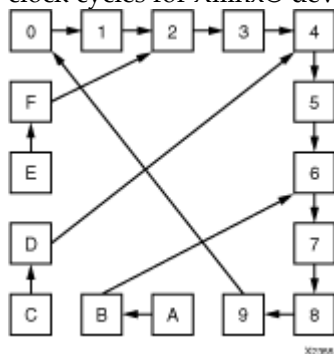
Macro: 4-Bit Cascadable BCD Counter with Clock Enable and Synchronous Reset



Introduction

CD4RE is a 4-bit (stage), synchronous resettable, cascadable binary-coded-decimal (BCD) counter. The synchronous reset input (R) is the highest priority input. When (R) is High, all other inputs are ignored; the (Q) outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock (C) transition. The (Q) outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when (CE) is Low. The (TC) output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs			Outputs					
R	CE	C	Q3	Q2	Q1	Q0	TC	CEO
1	X	↑	0	0	0	0	0	0
0	1	↑	Inc	Inc	Inc	Inc	TC	CEO

Inputs			Outputs					
R	CE	C	Q3	Q2	Q1	Q0	TC	CEO
0	0	X	No Change	No Change	No Change	No Change	TC	0
0	1	X	1	0	0	1	1	1
$TC = Q3 \cdot !Q2 \cdot !Q1 \cdot Q0$ $CEO = TC \cdot CE$								

Design Entry Method

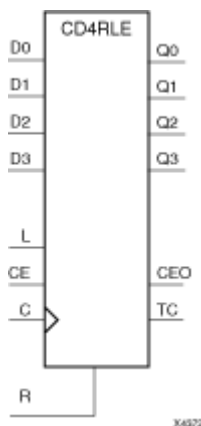
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CD4RLE

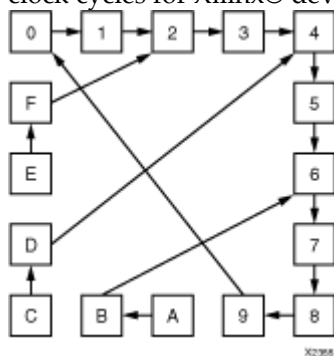
Macro: 4-Bit Loadable Cascadable BCD Counter with Clock Enable and Synchronous Reset



Introduction

CD4RLE is a 4-bit (stage), synchronous loadable, resettable, binary-coded-decimal (BCD) counter. The synchronous reset input (R) is the highest priority input. When R is High, all other inputs are ignored; the Q outputs, terminal count (TC), and clock enable out (CEO) go to logic level zero on the Low-to-High clock transitions. The data on the D inputs is loaded into the counter when the load enable input (L) is High during the Low-to-High clock (C) transition. The Q outputs increment when the clock enable input (CE) is High during the Low-to-High clock transition. The counter ignores clock transitions when CE is Low. The TC output is High when Q3 and Q0 are High and Q2 and Q1 are Low.

The counter recovers from any of six possible illegal states and returns to a normal count sequence within two clock cycles for Xilinx® devices, as shown in the following state diagram:



Create larger counters by connecting the CEO output of each stage to the CE input of the next stage and connecting the C, L, and R inputs in parallel. CEO is active (High) when TC and CE are High. The maximum length of the counter is determined by the accumulated CE-to-TC propagation delays versus the clock period. The clock period must be greater than $n(t_{CE-TC})$, where n is the number of stages and the time t_{CE-TC} is the CE-to-TC propagation delay of each stage. When cascading counters, use the CEO output if the counter uses the CE input or use the TC output if it does not.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs					Outputs					
R	L	CE	D3 – D0	C	Q3	Q2	Q1	Q0	TC	CEO
1	X	X	X	↑	0	0	0	0	0	0
0	1	X	D3 – D0	↑	D3	D	D	D0	TC	CEO
0	0	1	X	↑	Inc	Inc	Inc	Inc	TC	CEO
0	0	0	X	X	No Change	No Change	No Change	No Change	TC	0
0	0	1	X	X	1	0	0	1	1	1
$TC = Q3 \cdot !Q2 \cdot !Q1 \cdot Q0$ $CEO = TC \cdot CE$										

Design Entry Method

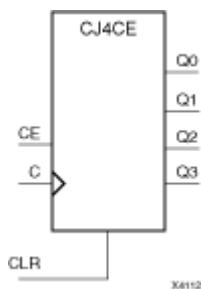
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CJ4CE

Macro: 4-Bit Johnson Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero, independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when (CE) is Low.

The Q3 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs	
CLR	CE	C	Q0	Q1 through Q3
1	X	X	0	0
0	0	X	No change	No change
0	1	↑	!q3	q0 through q2

q = state of referenced output one setup time prior to active clock transition

Design Entry Method

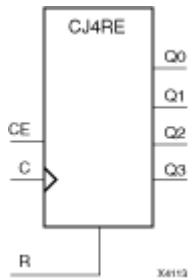
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CJ4RE

Macro: 4-Bit Johnson Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a resettable Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero during the Low-to-High clock (C) transition. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

The Q3 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs	
R	CE	C	Q0	Q1 through Q3
1	X	↑	0	0
0	0	X	No change	No change
0	1	↑	!q3	q0 through q2

q = state of referenced output one setup time prior to active clock transition

Design Entry Method

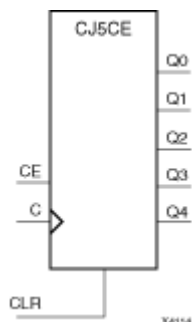
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CJ5CE

Macro: 5-Bit Johnson Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero, independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when (CE) is Low.

The Q4 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs			Outputs	
CLR	CE	C	Q0	Q1 through Q4
1	X	X	0	0
0	0	X	No change	No change
0	1	↑	!q4	q0 through q3

q = state of referenced output one setup time prior to active clock transition

Design Entry Method

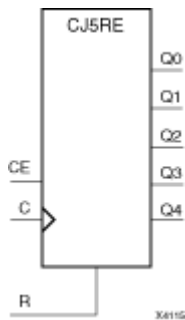
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CJ5RE

Macro: 5-Bit Johnson Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a resettable Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero during the Low-to-High clock (C) transition. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

The Q4 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs	
R	CE	C	Q0	Q1 through Q4
1	X	↑	0	0
0	0	X	No change	No change
0	1	↑	!q4	q0 through q3

q = state of referenced output one setup time prior to active clock transition

Design Entry Method

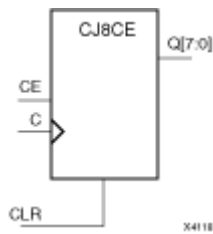
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CJ8CE

Macro: 8-Bit Johnson Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a clearable Johnson/shift counter. The asynchronous clear (CLR) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero, independent of clock (C) transitions. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when (CE) is Low.

The Q7 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs	
CLR	CE	C	Q0	Q1 through Q8
1	X	X	0	0
0	0	X	No change	No change
0	1	↑	!q7	q0 through q7

q = state of referenced output one setup time prior to active clock transition

Design Entry Method

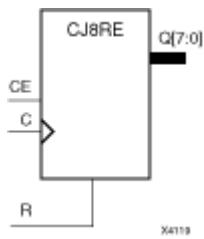
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CJ8RE

Macro: 8-Bit Johnson Counter with Clock Enable and Synchronous Reset



Introduction

This design element is a resettable Johnson/shift counter. The synchronous reset (R) input, when High, overrides all other inputs and forces the data (Q) outputs to logic level zero during the Low-to-High clock (C) transition. The counter increments (shifts Q0 to Q1, Q1 to Q2, and so forth) when the clock enable input (CE) is High during the Low-to-High clock transition. Clock transitions are ignored when CE is Low.

The Q7 output is inverted and fed back to input Q0 to provide continuous counting operation.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs	
R	CE	C	Q0	Q1 through Q7
1	X	↑	0	0
0	0	X	No change	No change
0	1	↑	!q7	q0 through q6

q = state of referenced output one setup time prior to active clock transition

Design Entry Method

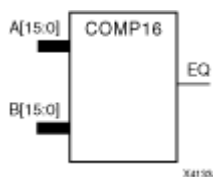
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

COMP16

Macro: 16-Bit Identity Comparator



Introduction

This design element is a 16-bit identity comparator. The equal output (EQ) is high when A15 – A0 and B15 – B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

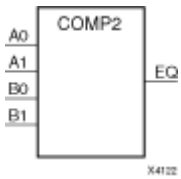
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

COMP2

Macro: 2-Bit Identity Comparator



Introduction

This design element is a 2-bit identity comparator. The equal output (EQ) is High when the two words A1 – A0 and B1 – B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

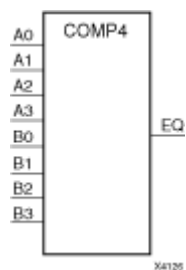
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

COMP4

Macro: 4-Bit Identity Comparator



Introduction

This design element is a 4-bit identity comparator. The equal output (EQ) is high when A3 – A0 and B3 – B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

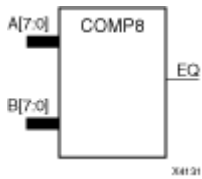
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

COMP8

Macro: 8-Bit Identity Comparator



Introduction

This design element is an 8-bit identity comparator. The equal output (EQ) is high when A7 – A0 and B7 – B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.

Design Entry Method

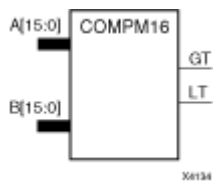
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

COMP16

Macro: 16-Bit Magnitude Comparator



Introduction

This design element is a 16-bit magnitude comparator that compare two positive Binary-weighted words. It compares A15 – A0 and B15 – B0, where A15 and B15 are the most significant bits.

The greater-than output (GT) is High when $A > B$, and the less-than output (LT) is High when $A < B$. When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

Inputs								Outputs	
A7, B7	A6, B6	A5, B5	A4, B4	A3, B3	A2, B2	A1, B1	A0, B0	GT	LT
A7>B7	X	X	X	X	X	X	X	1	0
A7<B7	X	X	X	X	X	X	X	0	1
A7=B7	A6>B6	X	X	X	X	X	X	1	0
A7=B7	A6<B6	X	X	X	X	X	X	0	1
A7=B7	A6=B6	A5>B5	X	X	X	X	X	1	0
A7=B7	A6=B6	A5<B5	X	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4>B4	X	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4<B4	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3>B3	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3<B3	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2>B2	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2<B2	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1>B1	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1<B1	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0>B0	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0<B0	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0=B0	0	0

Design Entry Method

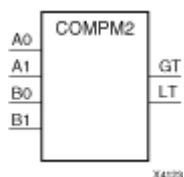
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

COMPM2

Macro: 2-Bit Magnitude Comparator



Introduction

This design element is a 2-bit magnitude comparator that compare two positive Binary-weighted words. It compares $A1 - A0$ and $B1 - B0$, where A1 and B1 are the most significant bits.

The greater-than output (GT) is High when $A > B$, and the less-than output (LT) is High when $A < B$. When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

Inputs				Outputs	
A1	B1	A0	B0	GT	LT
0	0	0	0	0	0
0	0	1	0	1	0
0	0	0	1	0	1
0	0	1	1	0	0
1	1	0	0	0	0
1	1	1	0	1	0
1	1	0	1	0	1
1	1	1	1	0	0
1	0	X	X	1	0
0	1	X	X	0	1

Design Entry Method

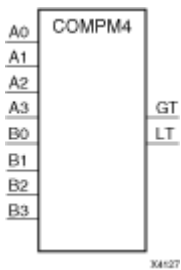
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

COMP4

Macro: 4-Bit Magnitude Comparator



Introduction

This design element is a 4-bit magnitude comparator that compare two positive Binary-weighted words. It compares $A3 - A0$ and $B3 - B0$, where $A3$ and $B3$ are the most significant bits.

The greater-than output (GT) is High when $A > B$, and the less-than output (LT) is High when $A < B$. When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

Inputs				Outputs	
A3, B3	A2, B2	A1, B1	A0, B0	GT	LT
$A3 > B3$	X	X	X	1	0
$A3 < B3$	X	X	X	0	1
$A3 = B3$	$A2 > B2$	X	X	1	0
$A3 = B3$	$A2 < B2$	X	X	0	1
$A3 = B3$	$A2 = B2$	$A1 > B1$	X	1	0
$A3 = B3$	$A2 = B2$	$A1 < B1$	X	0	1
$A3 = B3$	$A2 = A2$	$A1 = B1$	$A0 > B0$	1	0
$A3 = B3$	$A2 = B2$	$A1 = B1$	$A0 < B0$	0	1
$A3 = B3$	$A2 = B2$	$A1 = B1$	$A0 = B0$	0	0

Design Entry Method

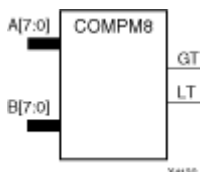
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

COMP8

Macro: 8-Bit Magnitude Comparator



Introduction

This design element is an 8-bit magnitude comparator that compare two positive Binary-weighted words. It compares A7 – A0 and B7 – B0, where A7 and B7 are the most significant bits.

The greater-than output (GT) is High when A > B, and the less-than output (LT) is High when A < B. When the two words are equal, both GT and LT are Low. Equality can be measured with this macro by comparing both outputs with a NOR gate.

Logic Table

Inputs								Outputs	
A7, B7	A6, B6	A5, B5	A4, B4	A3, B3	A2, B2	A1, B1	A0, B0	GT	LT
A7>B7	X	X	X	X	X	X	X	1	0
A7<B7	X	X	X	X	X	X	X	0	1
A7=B7	A6>B6	X	X	X	X	X	X	1	0
A7=B7	A6<B6	X	X	X	X	X	X	0	1
A7=B7	A6=B6	A5>B5	X	X	X	X	X	1	0
A7=B7	A6=B6	A5<B5	X	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4>B4	X	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4<B4	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3>B3	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3<B3	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2>B2	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2<B2	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1>B1	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1<B1	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0>B0	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0<B0	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0=B0	0	0

Design Entry Method

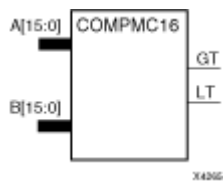
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

COMP16

Macro: 16-Bit Magnitude Comparator



Introduction

This design element is a 16-bit, magnitude comparator that compares two positive Binary weighted words A15 – A0 and B15 – B0, where A15 and B15 are the most significant bits.

This comparator is implemented using carry logic with relative location constraints to ensure efficient logic placement.

The greater-than output (GT) is High when $A > B$, and the less-than output (LT) is High when $A < B$. When the two words are equal, both GT and LT are Low. Equality can be flagged with this macro by connecting both outputs to a NOR gate.

Logic Table

Inputs								Outputs	
A7, B7	A6, B6	A5, B5	A4, B4	A3, B3	A2, B2	A1, B1	A0, B0	GT	LT
A7>B7	X	X	X	X	X	X	X	1	0
A7<B7	X	X	X	X	X	X	X	0	1
A7=B7	A6>B6	X	X	X	X	X	X	1	0
A7=B7	A6<B6	X	X	X	X	X	X	0	1
A7=B7	A6=B6	A5>B5	X	X	X	X	X	1	0
A7=B7	A6=B6	A5<B5	X	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4>B4	X	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4<B4	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3>B3	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3<B3	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2>B2	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2<B2	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1>B1	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1<B1	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0>B0	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0<B0	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0=B0	0	0

Design Entry Method

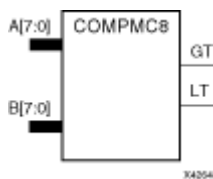
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

COMP8

Macro: 8-Bit Magnitude Comparator



Introduction

This design element is an 8-bit, magnitude comparator that compares two positive Binaryweighted words A7 – A0 and B7 – B0, where A7 and B7 are the most significant bits.

This comparator is implemented using carry logic with relative location constraints to ensure efficient logic placement.

The greater-than output (GT) is High when $A > B$, and the less-than output (LT) is High when $A < B$. When the two words are equal, both GT and LT are Low. Equality can be flagged with this macro by connecting both outputs to a NOR gate.

Logic Table

Inputs								Outputs	
A7, B7	A6, B6	A5, B5	A4, B4	A3, B3	A2, B2	A1, B1	A0, B0	GT	LT
A7>B7	X	X	X	X	X	X	X	1	0
A7<B7	X	X	X	X	X	X	X	0	1
A7=B7	A6>B6	X	X	X	X	X	X	1	0
A7=B7	A6<B6	X	X	X	X	X	X	0	1
A7=B7	A6=B6	A5>B5	X	X	X	X	X	1	0
A7=B7	A6=B6	A5<B5	X	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4>B4	X	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4<B4	X	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3>B3	X	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3<B3	X	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2>B2	X	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2<B2	X	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1>B1	X	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1<B1	X	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0>B0	1	0
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0<B0	0	1
A7=B7	A6=B6	A5=B5	A4=B4	A3=B3	A2=B2	A1=B1	A0=B0	0	0

Design Entry Method

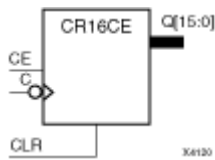
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CR16CE

Macro: 16-Bit Negative-Edge Binary Ripple Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is a 16-bit cascadable, clearable, binary ripple counter with clock enable and asynchronous clear.

Larger counters can be created by connecting the last Q output of the first stage to the clock input of the next stage. CLR and CE inputs are connected in parallel. The clock period is not affected by the overall length of a ripple counter. The overall clock-to-output propagation is $n(t_{C-Q})$, where n is the number of stages and the time t_{C-Q} is the C-to-Qz propagation delay of each stage.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
CLR	CE	C	Qz - Q0
1	X	X	0
0	0	X	No Change
0	1	∅	Inc

$z = \text{bit width} - 1$

Design Entry Method

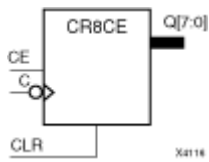
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

CR8CE

Macro: 8-Bit Negative-Edge Binary Ripple Counter with Clock Enable and Asynchronous Clear



Introduction

This design element is an 8-bit cascadable, clearable, binary, ripple counter with clock enable and asynchronous clear.

The asynchronous clear (CLR), when High, overrides all other inputs and causes the Q outputs to go to logic level zero. The counter increments when the clock enable input (CE) is High during the High-to-Low clock (C) transition. The counter ignores clock transitions when CE is Low.

Larger counters can be created by connecting the last Q output of the first stage to the clock input of the next stage. CLR and CE inputs are connected in parallel. The clock period is not affected by the overall length of a ripple counter. The overall clock-to-output propagation is $n(t_{C-Q})$, where n is the number of stages and the time t_{C-Q} is the C-to-Qz propagation delay of each stage.

This counter is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
CLR	CE	C	Qz - Q0
1	X	X	0
0	0	X	No Change
0	1	∅	Inc

$z = \text{bit width} - 1$

Design Entry Method

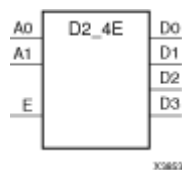
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

D2_4E

Macro: 2- to 4-Line Decoder/Demultiplexer with Enable



Introduction

This design element is a decoder/demultiplexer. When the enable (E) input of this element is High, one of four active-High outputs (D3 – D0) is selected with a 2-bit binary address (A1 – A0) input. The non-selected outputs are Low. Also, when the E input is Low, all outputs are Low. In demultiplexer applications, the E input is the data input.

Logic Table

Inputs			Outputs			
A1	A0	E	D3	D2	D1	D0
X	X	0	0	0	0	0
0	0	1	0	0	0	1
0	1	1	0	0	1	0
1	0	1	0	1	0	0
1	1	1	1	0	0	0

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

D3_8E

Macro: 3- to 8-Line Decoder/Demultiplexer with Enable



Introduction

When the enable (E) input of the D3_8E decoder/demultiplexer is High, one of eight active-High outputs (D7 – D0) is selected with a 3-bit binary address (A2 – A0) input. The non-selected outputs are Low. Also, when the E input is Low, all outputs are Low. In demultiplexer applications, the E input is the data input.

Logic Table

Inputs				Outputs							
A2	A1	A0	E	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	1
0	0	1	1	0	0	0	0	0	0	1	0
0	1	0	1	0	0	0	0	0	1	0	0
0	1	1	1	0	0	0	0	1	0	0	0
1	0	0	1	0	0	0	1	0	0	0	0
1	0	1	1	0	0	1	0	0	0	0	0
1	1	0	1	0	1	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0

Design Entry Method

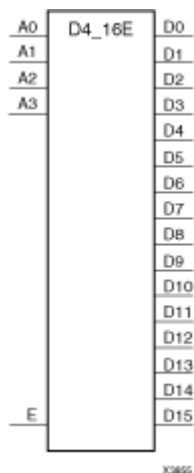
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

D4_16E

Macro: 4- to 16-Line Decoder/Demultiplexer with Enable



Introduction

This design element is a decoder/demultiplexer. When the enable (E) input of this design element is High, one of 16 active-High outputs (D15 – D0) is selected with a 4-bit binary address (A3 – A0) input. The non-selected outputs are Low. Also, when the E input is Low, all outputs are Low. In demultiplexer applications, the E input is the data input.

Design Entry Method

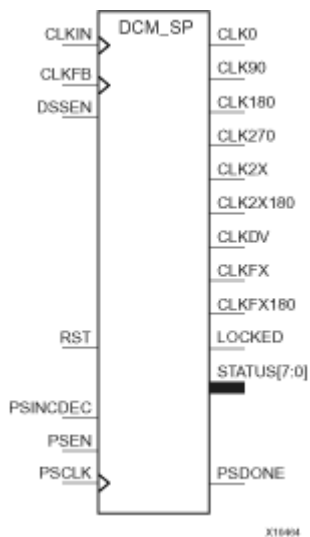
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

DCM_SP

Primitive: Digital Clock Manager



Introduction

This design element is a digital clock manager that provides multiple functions. It can implement a clock delay locked loop (DLL), a digital frequency synthesizer (DFS), and a digital phase shifter (DPS). DCM_SPs are useful for eliminating the clock delay coming on and off the chip, shifting the clock phase to improve data capture, deriving different frequency clocks, as well as other useful clocking functions.

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default
CLK_FEEDBACK	String	"NONE", "2X", or "1X"	"1X"
CLKDV_DIVIDE	REAL	1.5, 2.0, 2.5, 3.0, 3.5, 4.0, 4.5, 5.0, 5.5, 6.0, 6.5, 7.0, 7.5, 8.0, 9.0, 10.0, 11.0, 12.0, 13.0, 14.0, 15.0 or 16.0	2.0
CLKFX_DIVIDE	Integer	1 to 32	1
CLKFX_MULTIPLY	Integer	2 to 32	4
CLKIN_DIVIDE_BY_2	Boolean	FALSE, TRUE	FALSE
CLKIN_PERIOD	REAL	0.0001 to 1000	0
CLKOUT_PHASE_SHIFT	String	"NONE", "FIXED" or "VARIABLE"	"NONE"
DESKEW_ADJUST	String	"SOURCE_SYNCHRONOUS", "SYSTEM_SYNCHRONOUS" or "0"	""SYSTEM_SYNCHRONOUS"

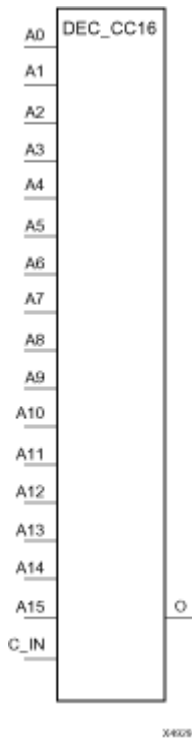
Attribute	Type	Allowed Values	Default
FACTORY_JF	16-Bit Hexadecimal	Any 16-Bit Hexadecimal value	C080
PHASE_SHIFT	Integer	-255 to 255	0
DFS_FREQUENCY_MODE	String	"LOW", "HIGH"	"LOW"
DLL_FREQUENCY_MODE	String	"LOW", "HIGH"	"LOW"
DSS_MODE	String	--	"NONE"
DUTY_CYCLE_CORRECTION	Boolean	TRUE, FALSE	TRUE
STARTUP_WAIT	Boolean	TRUE, FALSE	TRUE

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

DEC_CC16

Macro: 16-Bit Active Low Decoder



Introduction

This design element is a 16-bit decoder that is used to build wide-decoder functions. It is implemented by cascading CY_MUX elements driven by Look-Up Tables (LUTs). The C_IN pin can only be driven by the output (O) of a previous decode stage. When one or more of the inputs (A) are Low, the output is Low. When all the inputs are High and the C_IN input is High, the output is High. You can decode patterns by adding inverters to inputs.

Logic Table

Inputs					Outputs
A0	A1	...	Az	C_IN	O
1	1	1	1	1	1
X	X	X	X	0	0
0	X	X	X	X	0
X	0	X	X	X	0
X	X	X	0	X	0

z = 3 for DEC_CC4; z = 7 for DEC_CC8; z = 15 for DEC_CC16

Design Entry Method

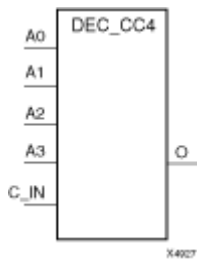
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

DEC_CC4

Macro: 4-Bit Active Low Decoder



Introduction

This design element is a 4-bit decoder that is used to build wide-decoder functions. It is implemented by cascading CY_MUX elements driven by Look-Up Tables (LUTs). The C_IN pin can only be driven by the output (O) of a previous decode stage. When one or more of the inputs (A) are Low, the output is Low. When all the inputs are High and the C_IN input is High, the output is High. You can decode patterns by adding inverters to inputs.

Logic Table

Inputs					Outputs
A0	A1	...	Az	C_IN	O
1	1	1	1	1	1
X	X	X	X	0	0
0	X	X	X	X	0
X	0	X	X	X	0
X	X	X	0	X	0

z = 3 for DEC_CC4; z = 7 for DEC_CC8; z = 15 for DEC_CC16

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

DEC_CC8

Macro: 8-Bit Active Low Decoder



Introduction

This design element is a 8-bit decoder that is used to build wide-decoder functions. It is implemented by cascading CY_MUX elements driven by Look-Up Tables (LUTs). The C_IN pin can only be driven by the output (O) of a previous decode stage. When one or more of the inputs (A) are Low, the output is Low. When all the inputs are High and the C_IN input is High, the output is High. You can decode patterns by adding inverters to inputs.

Logic Table

Inputs					Outputs
A0	A1	...	Az	C_IN	O
1	1	1	1	1	1
X	X	X	X	0	0
0	X	X	X	X	0
X	0	X	X	X	0
X	X	X	0	X	0

z = 3 for DEC_CC4; z = 7 for DEC_CC8; z = 15 for DEC_CC16

Design Entry Method

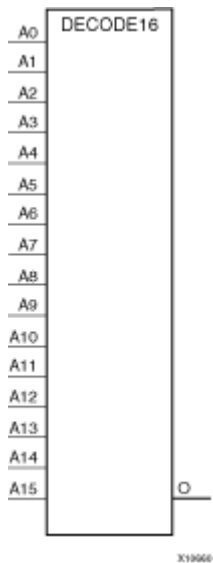
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

DECODE16

Macro: 16-Bit Active-Low Decoder



Introduction

In Spartan-3E, decoders are implemented using combinations of LUTs and MUXCYs.

Logic Table

Inputs				Outputs*
A0	A1	...	Az	O
1	1	1	1	1
0	X	X	X	0
X	0	X	X	0
X	X	X	0	0

z = bitwidth -1

*A pull-up resistor must be connected to the output to establish High-level drive current.

Design Entry Method

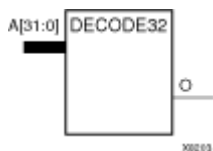
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

DECODE32

Macro: 32-Bit Active-Low Decoder



Introduction

This design element is a 32-bit active-low decoder that is implemented using combinations of LUTs and MUXCYs.

Logic Table

Inputs				Outputs
A0	A1	...	Az	O
1	1	1	1	1
0	X	X	X	0
X	0	X	X	0
X	X	X	0	0

z = 31 for DECODE32, z = 63 for DECODE64

Design Entry Method

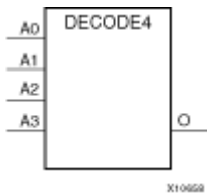
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

DECODE4

Macro: 4-Bit Active-Low Decoder



Introduction

In Spartan-3E, decoders are implemented using combinations of LUTs and MUXCYs.

Logic Table

Inputs				Outputs*
A0	A1	...	Az	O
1	1	1	1	1
0	X	X	X	0
X	0	X	X	0
X	X	X	0	0

z = bitwidth -1

*A pull-up resistor must be connected to the output to establish High-level drive current.

Design Entry Method

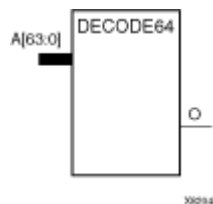
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

DECODE64

Macro: 64-Bit Active-Low Decoder



Introduction

This design element is a 64-bit active-low decoder that is implemented using combinations of LUTs and MUXCYs.

Logic Table

Inputs				Outputs
A0	A1	...	Az	O
1	1	1	1	1
0	X	X	X	0
X	0	X	X	0
X	X	X	0	0

z = 31 for DECODE32, z = 63 for DECODE64

Design Entry Method

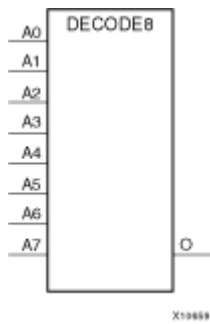
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

DECODE8

Macro: 8-Bit Active-Low Decoder



Introduction

In Spartan-3E, decoders are implemented using combinations of LUTs and MUXCYs.

Logic Table

Inputs				Outputs*
A0	A1	...	Az	O
1	1	1	1	1
0	X	X	X	0
X	0	X	X	0
X	X	X	0	0

z = bitwidth -1

*A pull-up resistor must be connected to the output to establish High-level drive current.

Design Entry Method

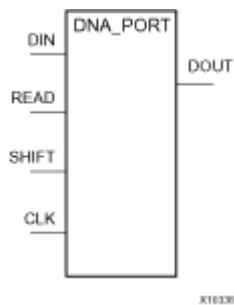
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

DNA_PORT

Primitive: Device DNA Data Access Port



Introduction

The DNA_PORT allows access to a dedicated shift register that can be loaded with the Device DNA data bits (unique ID) for a given Spartan-3A device. In addition to shifting out the DNA data bits, this component allows for the inclusion of supplemental data bits for additional data, or allows for the DNA data to rollover (repeat DNA data after initial data has been shifted out). This component is primarily used in conjunction with other circuitry to build added copy protection for the FPGA bitstream from possible theft.

Port Descriptions

Name	Direction	Width	Function
DOUT	Output	1-bit	Serial shifted output data
DIN	Input	1-bit	Your data input to the shift register
READ	Input	1-bit	Synchronous load of the shift register with the Device DNA data
SHIFT	Input	1-bit	Active high shift enable input
CLK	Input	1-bit	Clock Input

Design Entry Method

This design element can be used in schematics.

Connect all inputs and outputs to the design to ensure proper operation.

To access the Device DNA data, you must first load the shift register by setting the active high READ signal for one clock cycle. After the shift register is loaded, the data can be synchronously shifted out by enabling the active high SHIFT input and capturing the data out the DOUT output port. Additional data can be appended to the end of the 57-bit shift register by connecting the appropriate logic to the DIN port. If DNA data rollover is desired, connect the DOUT port directly to the DIN port to allow for the same data to be sifted out after completing the 57-bit shift operation. If no additional data is necessary, the DIN port can be tied to a logic zero. The attribute SIM_DNA_VALUE can be optionally set to allow for simulation of a possible DNA data sequence. By default, the Device DNA data bits are all zeros in the simulation model.

Available Attributes

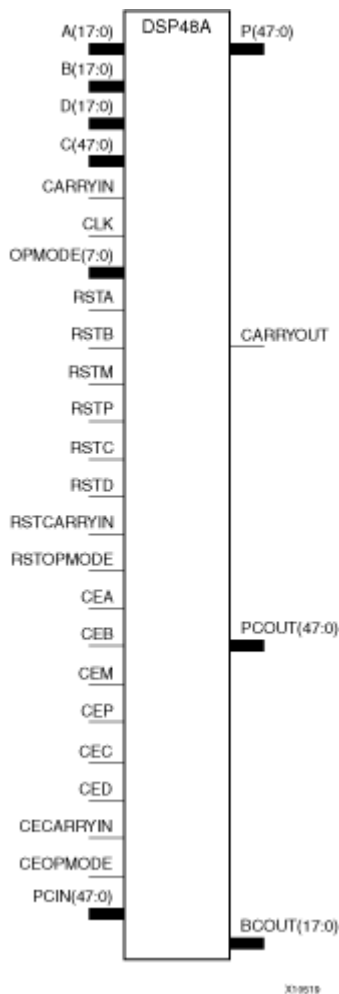
Attribute	Type	Allowed Values	Default	Description
SIM_DNA_VALUE	57-bit vector	Any 57-bit value	All zeros	Specifies a DNA value for simulation (device used)

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

DSP48A

Primitive: Multi-Functional, Cascadable, 48-bit Output, Arithmetic Block



Introduction

Note This element is available only for Spartan-3A DSP parts.

The DSP48A is a versatile, scalable, hard IP block that allows for the creation of compact, high-speed, arithmetic-intensive operations, such as those seen for many DSP algorithms. The block consists of a configurable, 18-bit, pre-add/sub, followed by an 18x18 signed multiplier, followed by a 48-bit post-add/sub/accum. Several configurable pipeline registers exist within the block, allowing for higher clock speeds with the trade-off of added latency. Opmode pins allow the block operation to change from one clock-cycle to the next, thus allowing a single block to serve several arithmetic functions within a design. Furthermore, multiple MSP1 blocks can be cascaded to efficiently form larger multiplication and addition functions.

Port Descriptions

Name	Direction	Width (Bits)	Function
Data Ports			
A	Input	18	18-bit data input to multiplier or post add/sub depending on the value of OPMODE[1:0]

Name	Direction	Width (Bits)	Function
B	Input	18	18-bit data input to multiplier, pre-add/sub and, perhaps, a post-add/sub depending on the value of OPMODE[3:0].
C	Input	48	48-bit data input to post-add/sub.
D	Input	18	18-bit data input to pre-add/sub.
CARRYIN	Input	1	External carry input to the post-add/sub. Should only be connected to the CARRYOUT pin of another DSP48A block.
P	Output	48	Primary data output.
CARRYOUT	Output	1	Carry out signal for post-add/sub. Should only be connected to the CARRYIN pin of another DSP48A.
Control Inputs			
CLK	Input	1	DSP48A clock
OPMODE	Input	8	Control input to select the arithmetic operations of the DSP48A.
OPMODE[1:0]			Specifies the source of the X input to the post-add/sub 0 - Specifies to place all zeroes (disable the post-add/sub). 1 - Use the POUT output signal. 2 - Use the concatenated D, B, A input signals. 3 - Use the multiplier product.
OPMODE[3:2]			Specifies the source of the Y input to the post-add/sub 0 - Specifies to place all zeroes (disable the post-add/sub and propagate the multiplier product to POUT). 1 - Use the PCIN. 2 - Use the POUT port (accumulator). 3 - Use the C port.
OPMODE[4]			Specifies the use of the pre-add/sub 0 - Selects to use the pre-adder adding or subtracting the values on the B and D ports prior to the multiplier. 1 - Bypass the pre-adder, supplying the data on Port B directly to the multiplier.
OPMODE[5]			Force a value on carry-in to the post-adder. Only applicable when CARRYINSEL = "OPMODE5".
OPMODE[6]			Specifies whether the pre-add/sub is an adder or subtracter 0 - Specifies pre-add/sub to perform an addition operation. 1 - Specifies pre-add/sub to perform a subtract operation.
OPMODE[7]			Specifies whether the post-add/sub is an adder or subtracter 0 - Specifies post-add/sub to perform an addition operation. 1 - Specifies post-add/sub to perform a subtract operation.
Reset/Clock Enable Inputs			

Name	Direction	Width (Bits)	Function
RSTA	Input	1	Active high, reset for the A port registers (AREG=1 or 2). Tie to logic zero if not used. This reset is configurable to be synchronous or asynchronous, depending on the value of the RSTTYPE attribute.
RSTB	Input	1	Active high, reset for the B port registers (BREG!="NONE"). Tie to logic zero if not used. This reset is configurable to be synchronous or asynchronous depending on the value of the RSTTYPE attribute.
RSTC	Input	1	Active high, reset for the C input registers (CREG=1). Tie to logic zero if not used. This reset is configurable to be synchronous or asynchronous depending on the value of the RSTTYPE attribute.
RSTD	Input	1	Active high, reset for the D port registers (DREG=1). Tie to logic zero if not used. This reset is configurable to be synchronous or asynchronous depending on the value of the RSTTYPE attribute.
RSTM	Input	1	Active high, reset for the multiplier registers (MREG=1). Tie to logic zero if not used. This reset is configurable to be synchronous or asynchronous depending on the value of the RSTTYPE attribute.
RSTP	Input	1	Active high, reset for the P output registers (PREG=1). Tie to logic zero if not used. This reset is configurable to be synchronous or asynchronous depending on the value of the RSTTYPE attribute.
RSTCARRYIN	Input	1	Active high, reset for the carry-in register (CARRYINREG =1). Tie to logic zero if not used. This reset is configurable to be synchronous or asynchronous depending on the value of the RSTTYPE attribute.
RSTOPMODE	Input	1	Active high, reset for the OPMODE registers (OPMODEREG=1). Tie to logic zero if not used. This reset is configurable to be synchronous or asynchronous depending on the value of the RSTTYPE attribute.
CEA	Input	1	Active high, clock enable for the A port registers (AREG=1 or 2). Tie to logic one if not used and AREG=1 or 2. Tie to logic zero if AREG=0.
CEB	Input	1	Active high, clock enable for the B port registers (BREG!="NONE"). Tie to logic one if not used and BREG!="NONE". Tie to logic zero if BREG="NONE".
CEC	Input	1	Active high, clock enable for the C port registers (CREG=1). Tie to logic one if not used and CREG=1. Tie to a logic zero if CREG=0..
CED	Input	1	Active high, clock enable for the D port registers (DREG=1). Tie to logic one if not used and DREG=1. Tie to a logic zero if DREG=0.
CEM	Input	1	Active high, clock enable for the multiplier registers (MREG=1). Tie to logic one if not used and MREG=1. Tie to a logic zero if MREG=0.
CEP	Input	1	Active high, clock enable for the output port registers (PREG=1). Tie to logic one if not used and PREG=1. Tie to a logic zero if PREG=0.
CECARRYIN	Input	1	Active high, clock enable for the carry-in registers (CARRYINREG=1). Tie to logic one if not used and CARRYINREG=1. Tie to a logic zero if CARRINREG=0.
CEOPMODE	Input	1	Clock enable for the OPMODE input registers (OPMODEREG=1). Tie to logic one if not used and OPMODEREG=1. Tie to a logic zero if OPMODEREG=0.
Cascade Ports			
PCIN	Input	48	Cascade input for Port P. If used, connect to PCOUT of upstream cascaded DSP48A. If not used, tie port to all zeros.
PCOUT	Output	48	Cascade output for Port P. If used, connect to PCIN of downstream cascaded DSP48A. If not used, leave unconnected.
BCOUT	Output	18	Cascade output for Port B. If used, connect to the B port of downstream cascaded DSP48A. If not used, leave unconnected.

Design Entry Method

This design element can be used in schematics.

Available Attributes

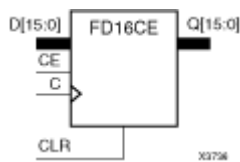
Attribute	Type	Allowed Values	Default	Description
A0REG	Integer	0 or 1	0	Specifies to enable/disable the first pipeline stage on the
A1REG	Integer	0 or 1	1	Specifies to enable/disable the second pipeline stage on the
B0REG	Integer	0 or 1	0	Specifies to enable/disable the first pipeline stage on the
B1REG	Integer	0 or 1	1	Specifies to enable/disable the second pipeline stage on the
CARRYINREG	Integer	0 or 1	1	Selects whether to register the CARRYIN input to the DSP48A. This should only be used when CARRYINSEL is set to "CARRYIN". If CARRYINSEL is set to "CARRYIN", the CARRYIN pin is used.
CARRYINSEL	String	"CARRYIN", "OPMODE5"	"CARRYIN"	Selects whether the post add/sub carry-in signal should be registered. The CARRYIN pin (connected to the CARRYOUT of a DSP48A) should be used when CARRYINSEL is set to "CARRYIN". The signal should be dynamically controlled from the FPGA fabric by the CARRYIN pin.
CREG	Integer	0 or 1	1	Selects whether to register the C input to the DSP48A.
DREG	Integer	0 or 1	1	Selects whether to register the D input to the DSP48A.
MREG	Integer	0 or 1	1	Selects whether to register the multiplier stage of the DSP48A.
OPMODEREG	Integer	0 or 1	1	Selects whether to register the OPMODE inputs to the DSP48A.
PREG	Integer	0 or 1	1	Selects whether to register the P output of the DSP48A.
RSTTYPE	String	ASYNC", "SYNC"	"SYNC"	Selects whether all resets for the DSP48A should have synchronous or asynchronous reset capability. Due to improved timing stability, it is recommended to always have this set to "SYNC". If "ASYNC" is selected, asynchronous reset is absolutely necessary.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FD16CE

Macro: 16-Bit Data Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a 16-bit data register with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
CLR	CE	Dz – D0	C	Qz – Q0
1	X	X	X	0
0	0	X	X	No Change
0	1	Dn	↑	Dn

z = bit-width - 1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

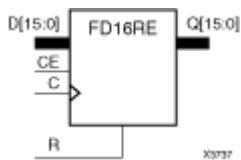
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	16-bit Binary	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FD16RE

Macro: 16-Bit Data Register with Clock Enable and Synchronous Reset



Introduction

This design element is a 16-bit data registers. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
R	CE	Dz – D0	C	Qz – Q0
1	X	X	↑	0
0	0	X	X	No Change
0	1	Dn	↑	Dn

z = bit-width - 1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

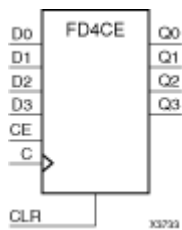
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	16-bit Binary	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FD4CE

Macro: 4-Bit Data Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a 4-bit data register with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
CLR	CE	D _z – D0	C	Q _z – Q0
1	X	X	X	0
0	0	X	X	No Change
0	1	D _n	↑	D _n

z = bit-width - 1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

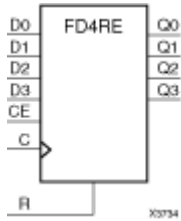
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	4-bit Binary	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FD4RE

Macro: 4-Bit Data Register with Clock Enable and Synchronous Reset



Introduction

This design element is a 4-bit data registers. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q0) during the Low-to-High clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs				Outputs
R	CE	Dz – D0	C	Qz – Q0
1	X	X	↑	0
0	0	X	X	No Change
0	1	Dn	↑	Dn

z = bit-width - 1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

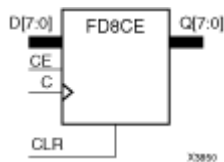
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	4-bit Binary	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FD8CE

Macro: 8-Bit Data Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a 8-bit data register with clock enable and asynchronous clear. When clock enable (CE) is High and asynchronous clear (CLR) is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High clock (C) transition. When CLR is High, it overrides all other inputs and resets the data outputs (Q) Low. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
CLR	CE	Dz - D0	C	Qz - Q0
1	X	X	X	0
0	0	X	X	No Change
0	1	Dn	↑	Dn

z = bit-width - 1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

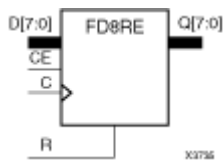
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	8-bit Binary	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FD8RE

Macro: 8-Bit Data Register with Clock Enable and Synchronous Reset



Introduction

This design element is an 8-bit data register. When the clock enable (CE) input is High, and the synchronous reset (R) input is Low, the data on the data inputs (D) is transferred to the corresponding data outputs (Q) during the Low-to-High clock (C) transition. When R is High, it overrides all other inputs and resets the data outputs (Q) Low on the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
R	CE	Dz – D0	C	Qz – Q0
1	X	X	↑	0
0	0	X	X	No Change
0	1	Dn	↑	Dn

z = bit-width - 1

Design Entry Method

This design element is only for use in schematics.

Available Attributes

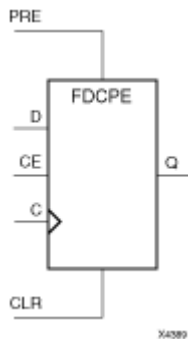
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 8-Bit Value	All zeros	Sets the initial value of Q output after configuration.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FDCPE

Primitive: D Flip-Flop with Clock Enable and Asynchronous Preset and Clear



Introduction

This design element is a single D-type flip-flop with data (D), clock enable (CE), asynchronous preset (PRE), and asynchronous clear (CLR) inputs. The asynchronous active high PRE sets the Q output High; that active high CLR resets the output Low and has precedence over the PRE input. Data on the D input is loaded into the flip-flop when PRE and CLR are Low and CE is High on the Low-to-High clock (C) transition. When CE is Low, the clock transitions are ignored and the previous value is retained. The FDCPE is generally implemented as a slice or IOB register within the device.

For FPGA devices, upon power-up, the initial value of this component is specified by the INIT attribute. If a subsequent GSR (Global Set/Reset) is asserted, the flop is asynchronously set to the INIT value.

Note While this device supports the use of asynchronous set and reset, it is not generally recommended to be used for in most cases. Use of asynchronous signals pose timing issues within the design that are difficult to detect and control and also have an adverse affect on logic optimization causing a larger design that can consume more power than if a synchronous set or reset is used.

Logic Table

Inputs					Outputs
CLR	PRE	CE	D	C	Q
1	X	X	X	X	0
0	1	X	X	X	1
0	0	0	X	X	No Change
0	0	1	D	↑	D

Port Descriptions

Name	Direction	Width	Function
Q	Output	1-Bit	Data output
C	Input	1-Bit	Clock input
CE	Input	1-Bit	Clock enable input
CLR	Input	1-Bit	Asynchronous clear input
D	Input	1-Bit	Data input
PRE	Input	1-Bit	Asynchronous set input

Design Entry Method

This design element can be used in schematics.

Available Attributes

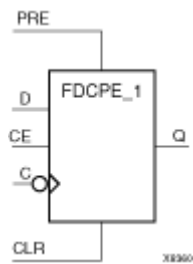
Attribute	Type	Allowed Values	Default	Description
INIT	1-Bit Binary	0 or 1	0	Sets the initial value of Q output after configuration and on GSR

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FDCPE_1

Primitive: D Flip-Flop with Negative-Edge Clock, Clock Enable, and Asynchronous Preset and Clear



Introduction

FDCPE_1 is a single D-type flip-flop with data (D), clock enable (CE), asynchronous preset (PRE), and asynchronous clear (CLR) inputs and data output (Q). The asynchronous PRE, when High, sets the (Q) output High; CLR, when High, resets the output Low. Data on the (D) input is loaded into the flip-flop when PRE and CLR are Low and CE is High on the High-to-Low clock (C) transition. When CE is Low, the clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs					Outputs
CLR	PRE	CE	D	C	Q
1	X	X	X	X	0
0	1	X	X	X	1
0	0	0	X	X	No Change
0	0	1	D	↓	D

Port Descriptions

Name	Direction	Width	Function
Q	Output	1-Bit	Data output
C	Input	1-Bit	Clock input
CE	Input	1-Bit	Clock enable input
CLR	Input	1-Bit	Asynchronous clear input
D	Input	1-Bit	Data input
PRE	Input	1-Bit	Asynchronous set input

Design Entry Method

This design element can be used in schematics.

Available Attributes

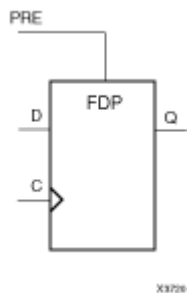
Attribute	Type	Allowed Values	Default	Description
INIT	1-Bit Binary	0 or 1	0	Sets the initial value of Q output after configuration

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FDP

Primitive: D Flip-Flop with Asynchronous Preset



Introduction

This design element is a single D-type flip-flop with data (D) and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and presets the (Q) output High. The data on the (D) input is loaded into the flip-flop when PRE is Low on the Low-to-High clock (C) transition.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
PRE	C	D	Q
1	X	X	1
0	↑	D	D
0	↑	0	0

Design Entry Method

This design element is only for use in schematics.

Available Attributes

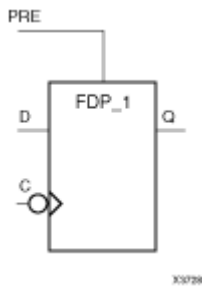
Attribute	Type	Allowed Values	Default	Description
INIT	1-Bit Binary	0 or 1	0	Sets the initial value of Q output after configuration

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FDP_1

Primitive: D Flip-Flop with Negative-Edge Clock and Asynchronous Preset



Introduction

This design element is a single D-type flip-flop with data (D) and asynchronous preset (PRE) inputs and data output (Q). The asynchronous PRE, when High, overrides all other inputs and presets the Q output High. The data on the D input is loaded into the flip-flop when PRE is Low on the High-to-Low clock (C) transition.

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
PRE	C	D	Q
1	X	X	1
0	↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

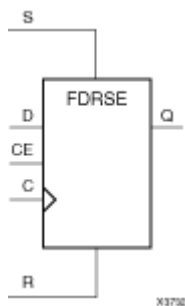
Attribute	Type	Allowed Values	Default	Description
INIT	1-Bit Binary	0 or 1	0	Sets the initial value of Q output after configuration

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FDRSE

Primitive: D Flip-Flop with Synchronous Reset and Set and Clock Enable



Introduction

FDRSE is a single D-type flip-flop with synchronous reset (R), synchronous set (S), clock enable (CE) inputs. The reset (R) input, when High, overrides all other inputs and resets the Q output Low during the Low-to-High clock transition. (Reset has precedence over Set.) When the set (S) input is High and R is Low, the flip-flop is set, output High, during the Low-to-High clock (C) transition. Data on the D input is loaded into the flip-flop when R and S are Low and CE is High during the Low-to-High clock transition.

Upon power-up, the initial value of this component is specified by the INIT attribute. If a subsequent GSR (Global Set/Reset) is asserted, the flop is asynchronously set to the INIT value.

Logic Table

Inputs					Outputs
R	S	CE	D	C	Q
1	X	X	X	↑	0
0	1	X	X	↑	1
0	0	0	X	X	No Change
0	0	1	1	↑	1
0	0	1	0	↑	0

Design Entry Method

This design element can be used in schematics.

Available Attributes

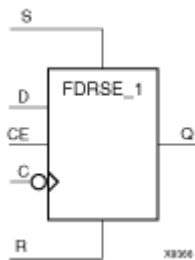
Attribute	Type	Allowed Values	Default	Description
INIT	1-Bit Binary	0 or 1	0	Sets the initial value of Q output after configuration and on GSR.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FDRSE_1

Primitive: D Flip-Flop with Negative-Clock Edge, Synchronous Reset and Set, and Clock Enable



Introduction

FDRSE_1 is a single D-type flip-flop with synchronous reset (R), synchronous set (S), and clock enable (CE) inputs and data output (Q). The reset (R) input, when High, overrides all other inputs and resets the (Q) output Low during the High-to-Low clock transition. (Reset has precedence over Set.) When the set (S) input is High and R is Low, the flip-flop is set, output High, during the High-to-Low clock (C) transition. Data on the (D) input is loaded into the flip-flop when (R) and (S) are Low and (CE) is High during the High-to-Low clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs					Outputs
R	S	CE	D	C	Q
1	X	X	X	↓	0
0	1	X	X	↓	1
0	0	0	X	X	No Change
0	0	1	D	↓	D

Design Entry Method

This design element can be used in schematics.

Available Attributes

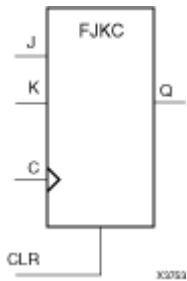
Attribute	Type	Allowed Values	Default	Description
INIT	1-Bit Binary	0 or 1	0	Sets the initial value of Q output after configuration and on GSR.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FJKC

Macro: J-K Flip-Flop with Asynchronous Clear



Introduction

This design element is a single J-K-type flip-flop with J, K, and asynchronous clear (CLR) inputs and data output (Q). The asynchronous clear (CLR) input, when High, overrides all other inputs and resets the Q output Low. When CLR is Low, the output responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock (C) transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs				Outputs
CLR	J	K	C	Q
1	X	X	X	0
0	0	0	↑	No Change
0	0	1	↑	0
0	1	0	↑	1
0	1	1	↑	Toggle

Design Entry Method

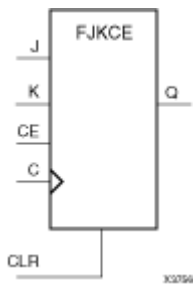
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FJKCE

Macro: J-K Flip-Flop with Clock Enable and Asynchronous Clear



Introduction

This design element is a single J-K-type flip-flop with J, K, clock enable (CE), and asynchronous clear (CLR) inputs and data output (Q). The asynchronous clear (CLR), when High, overrides all other inputs and resets the Q output Low. When CLR is Low and CE is High, Q responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock transition. When CE is Low, the clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs					Outputs
CLR	CE	J	K	C	Q
1	X	X	X	X	0
0	0	X	X	X	No Change
0	1	0	0	X	No Change
0	1	0	1	↑	0
0	1	1	0	↑	1
0	1	1	1	↑	Toggle

Design Entry Method

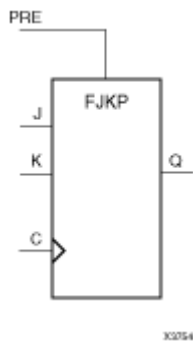
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FJKP

Macro: J-K Flip-Flop with Asynchronous Preset



Introduction

This design element is a single J-K-type flip-flop with J, K, and asynchronous preset (PRE) inputs and data output (Q). The asynchronous preset (PRE) input, when High, overrides all other inputs and sets the (Q) output High. When (PRE) is Low, the (Q) output responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock transition.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
PRE	J	K	C	Q
1	X	X	X	1
0	0	0	X	No Change
0	0	1	↑	0
0	1	0	↑	1
0	1	1	↑	Toggle

Design Entry Method

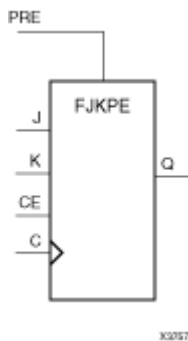
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FJKPE

Macro: J-K Flip-Flop with Clock Enable and Asynchronous Preset



Introduction

This design element is a single J-K-type flip-flop with J, K, clock enable (CE), and asynchronous preset (PRE) inputs and data output (Q). The asynchronous preset (PRE), when High, overrides all other inputs and sets the (Q) output High. When (PRE) is Low and (CE) is High, the (Q) output responds to the state of the J and K inputs, as shown in the logic table, during the Low-to-High clock (C) transition. When (CE) is Low, clock transitions are ignored.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs					Outputs
PRE	CE	J	K	C	Q
1	X	X	X	X	1
0	0	X	X	X	No Change
0	1	0	0	X	No Change
0	1	0	1	↑	0
0	1	1	0	↑	1
0	1	1	1	↑	Toggle

Design Entry Method

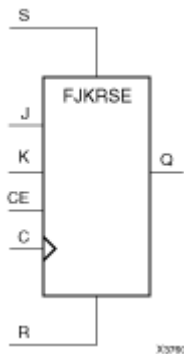
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FJKRSE

Macro: J-K Flip-Flop with Clock Enable and Synchronous Reset and Set



Introduction

This design element is a single J-K-type flip-flop with J, K, synchronous reset (R), synchronous set (S), and clock enable (CE) inputs and data output (Q). When synchronous reset (R) is High during the Low-to-High clock (C) transition, all other inputs are ignored and output (Q) is reset Low. When synchronous set (S) is High and (R) is Low, output (Q) is set High. When (R) and (S) are Low and (CE) is High, output (Q) responds to the state of the J and K inputs, according to the following logic table, during the Low-to-High clock (C) transition. When (CE) is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs						Outputs
R	S	CE	J	K	C	Q
1	X	X	X	X	↑	0
0	1	X	X	X	↑	1
0	0	0	X	X	X	No Change
0	0	1	0	0	X	No Change
0	0	1	0	1	↑	0
0	0	1	1	1	↑	Toggle
0	0	1	1	0	↑	1

Design Entry Method

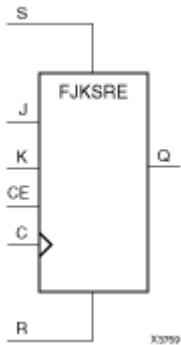
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FJKSRE

Macro: J-K Flip-Flop with Clock Enable and Synchronous Set and Reset



Introduction

This design element is a single J-K-type flip-flop with J, K, synchronous set (S), synchronous reset (R), and clock enable (CE) inputs and data output (Q). When synchronous set (S) is High during the Low-to-High clock (C) transition, all other inputs are ignored and output (Q) is set High. When synchronous reset (R) is High and (S) is Low, output (Q) is reset Low. When (S) and (R) are Low and (CE) is High, output (Q) responds to the state of the J and K inputs, as shown in the following logic table, during the Low-to-High clock (C) transition. When (CE) is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs						Outputs
S	R	CE	J	K	C	Q
1	X	X	X	X	↑	1
0	1	X	X	X	↑	0
0	0	0	X	X	X	No Change
0	0	1	0	0	X	No Change
0	0	1	0	1	↑	0
0	0	1	1	0	↑	1
0	0	1	1	1	↑	Toggle

Design Entry Method

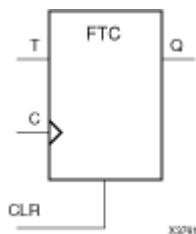
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FTC

Macro: Toggle Flip-Flop with Asynchronous Clear



Introduction

This design element is a synchronous, resettable toggle flip-flop. The asynchronous clear (CLR) input, when High, overrides all other inputs and resets the data output (Q) Low. The (Q) output toggles, or changes state, when the toggle enable (T) input is High and (CLR) is Low during the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
CLR	T	C	Q
1	X	X	0
0	0	X	No Change
0	1	↑	Toggle

Design Entry Method

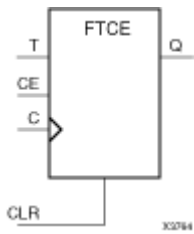
You can instantiate this element when targeting a CPLD, but not when you are targeting an FPGA.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FTCE

Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Clear



Introduction

This design element is a toggle flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear (CLR) input is High, all other inputs are ignored and the data output (Q) is reset Low. When CLR is Low and toggle enable (T) and clock enable (CE) are High, Q output toggles, or changes state, during the Low-to-High clock (C) transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs				Outputs
CLR	CE	T	C	Q
1	X	X	X	0
0	0	X	X	No Change
0	1	0	X	No Change
0	1	1	↑	Toggle

Design Entry Method

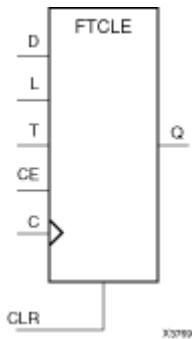
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FTCLE

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear



Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear input (CLR) is High, all other inputs are ignored and output Q is reset Low. When load enable input (L) is High and CLR is Low, clock enable (CE) is overridden and the data on data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When toggle enable (T) and CE are High and L and CLR are Low, output Q toggles, or changes state, during the Low- to-High clock transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs						Outputs
CLR	L	CE	T	D	C	Q
1	X	X	X	X	X	0
0	1	X	X	D	↑	D
0	0	0	X	X	X	No Change
0	0	1	0	X	X	No Change
0	0	1	1	X	↑	Toggle

Design Entry Method

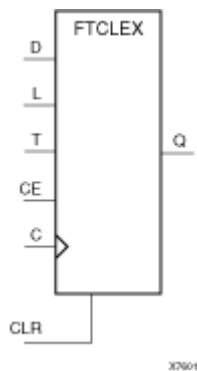
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FTCLEX

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Clear



Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and asynchronous clear. When the asynchronous clear input (CLR) is High, all other inputs are ignored and output Q is reset Low. When load enable input (L) is High, CLR is Low, and CE is High, the data on data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When toggle enable (T) and CE are High and L and CLR are Low, output Q toggles, or changes state, during the Low- to-High clock transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs						Outputs
CLR	L	CE	T	D	C	Q
1	X	X	X	X	X	0
0	1	X	X	D	↑	D
0	0	0	X	X	X	No Change
0	0	1	0	X	X	No Change
0	0	1	1	X	↑	Toggle

Design Entry Method

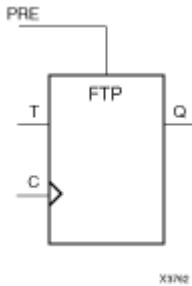
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FTP

Macro: Toggle Flip-Flop with Asynchronous Preset



Introduction

This design element is a toggle flip-flop with toggle enable and asynchronous preset. When the asynchronous preset (PRE) input is High, all other inputs are ignored and output (Q) is set High. When toggle-enable input (T) is High and (PRE) is Low, output (Q) toggles, or changes state, during the Low-to-High clock (C) transition.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
PRE	T	C	Q
1	X	X	1
0	0	X	No Change
0	1	↑	Toggle

Design Entry Method

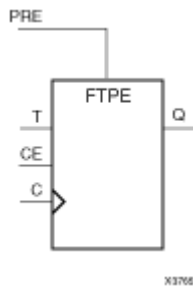
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FTPE

Macro: Toggle Flip-Flop with Clock Enable and Asynchronous Preset



Introduction

This design element is a toggle flip-flop with toggle and clock enable and asynchronous preset. When the asynchronous preset (PRE) input is High, all other inputs are ignored and output (Q) is set High. When the toggle enable input (T) is High, clock enable (CE) is High, and (PRE) is Low, output (Q) toggles, or changes state, during the Low-to-High clock transition. When (CE) is Low, clock transitions are ignored.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
PRE	CE	T	C	Q
1	X	X	X	1
0	0	X	X	No Change
0	1	0	X	No Change
0	1	1	↑	Toggle

Design Entry Method

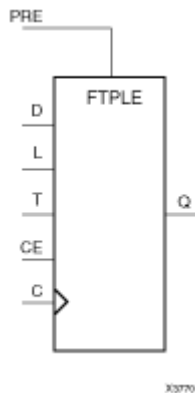
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FTPLE

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Asynchronous Preset



Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and asynchronous preset. When the asynchronous preset input (PRE) is High, all other inputs are ignored and output (Q) is set High. When the load enable input (L) is High and (PRE) is Low, the clock enable (CE) is overridden and the data (D) is loaded into the flip-flop during the Low-to-High clock transition. When L and PRE are Low and toggle-enable input (T) and (CE) are High, output (Q) toggles, or changes state, during the Low-to-High clock transition. When (CE) is Low, clock transitions are ignored.

For FPGA devices, this flip-flop is asynchronously preset, output High, when power is applied. Power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs						Outputs
PRE	L	CE	T	D	C	Q
1	X	X	X	X	X	1
0	1	X	X	D	?	D
0	0	0	X	X	X	No Change
0	0	1	0	X	X	No Change
0	0	1	1	X	?	Toggle

Design Entry Method

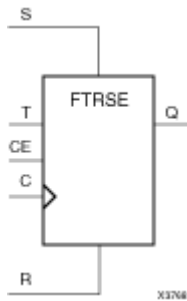
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FTRSE

Macro: Toggle Flip-Flop with Clock Enable and Synchronous Reset and Set



Introduction

This design element is a toggle flip-flop with toggle and clock enable and synchronous reset and set. When the synchronous reset input (R) is High, it overrides all other inputs and the data output (Q) is reset Low. When the synchronous set input (S) is High and (R) is Low, clock enable input (CE) is overridden and output (Q) is set High. (Reset has precedence over Set.) When toggle enable input (T) and (CE) are High and (R) and (S) are Low, output (Q) toggles, or changes state, during the Low-to-High clock transition.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs					Outputs
R	S	CE	T	C	Q
1	X	X	X	↑	0
0	1	X	X	↑	1
0	0	0	X	X	No Change
0	0	1	0	X	No Change
0	0	1	1	↑	Toggle

Design Entry Method

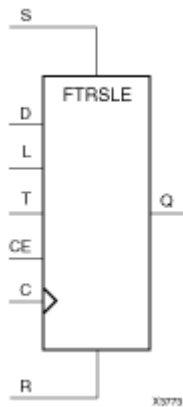
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FTRSLE

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Synchronous Reset and Set



Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and synchronous reset and set. The synchronous reset input (R), when High, overrides all other inputs and resets the data output (Q) Low. (Reset has precedence over Set.) When R is Low and synchronous set input (S) is High, the clock enable input (CE) is overridden and output Q is set High. When R and S are Low and load enable input (L) is High, CE is overridden and data on data input (D) is loaded into the flip-flop during the Low-to-High clock transition. When R, S, and L are Low, CE is High and T is High, output Q toggles, or changes state, during the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs							Outputs
R	S	L	CE	T	D	C	Q
1	0	X	X	X	X	↑	0
0	1	X	X	X	X	↑	1
0	0	1	X	X	1	↑	1
0	0	1	X	X	0	↑	0
0	0	0	0	X	X	X	No Change
0	0	0	1	0	X	X	No Change
0	0	0	1	1	X	↑	Toggle

Design Entry Method

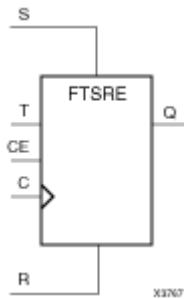
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FTSRE

Macro: Toggle Flip-Flop with Clock Enable and Synchronous Set and Reset



Introduction

This design element is a toggle flip-flop with toggle and clock enable and synchronous set and reset. The synchronous set input, when High, overrides all other inputs and sets data output (Q) High. (Set has precedence over Reset.) When synchronous reset input (R) is High and S is Low, clock enable input (CE) is overridden and output Q is reset Low. When toggle enable input (T) and CE are High and S and R are Low, output Q toggles, or changes state, during the Low-to-High clock transition. When CE is Low, clock transitions are ignored.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs					Outputs
S	R	CE	T	C	Q
1	X	X	X	↑	1
0	1	X	X	↑	0
0	0	0	X	X	No Change
0	0	1	0	X	No Change
0	0	1	1	↑	Toggle

Design Entry Method

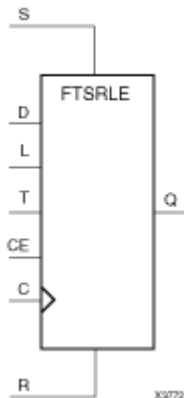
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

FTSRLE

Macro: Toggle/Loadable Flip-Flop with Clock Enable and Synchronous Set and Reset



Introduction

This design element is a toggle/loadable flip-flop with toggle and clock enable and synchronous set and reset. The synchronous set input (S), when High, overrides all other inputs and sets data output (Q) High. (Set has precedence over Reset.) When synchronous reset (R) is High and (S) is Low, clock enable input (CE) is overridden and output (Q) is reset Low. When load enable input (L) is High and S and R are Low, CE is overridden and data on data input (D) is loaded into the flip-flop during the Low-to-High clock transition. When the toggle enable input (T) and (CE) are High and (S), (R), and (L) are Low, output (Q) toggles, or changes state, during the Low-to-High clock transition. When (CE) is Low, clock transitions are ignored.

For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs							Outputs
S	R	L	CE	T	D	C	Q
1	X	X	X	X	X	↑	1
0	1	X	X	X	X	↑	0
0	0	1	X	X	1	↑	1
0	0	1	X	X	0	↑	0
0	0	0	0	X	X	X	No Change
0	0	0	1	0	X	X	No Change
0	0	0	1	1	X	↑	Toggle

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

GND

Primitive: Ground-Connection Signal Tag



Introduction

The GND signal tag, or parameter, forces a net or input function to a Low logic level. A net tied to GND cannot have any other source.

When the logic-trimming software or fitter encounters a net or input function tied to GND, it removes any logic that is disabled by the GND signal. The GND signal is only implemented when the disabled logic cannot be removed.

Design Entry Method

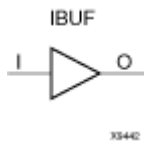
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IBUF

Primitive: Input Buffer



Introduction

This design element is automatically inserted (inferred) by the synthesis tool to any signal directly connected to a top-level input or in-out port of the design. You should generally let the synthesis tool infer this buffer. However, it can be instantiated into the design if required. In order to do so, connect the input port (I) directly to the associated top-level input or in-out port, and connect the output port (O) to the logic sourced by that port. Modify any necessary generic maps (VHDL) or named parameter value assignment (Verilog) in order to change the default behavior of the component.

Port Descriptions

Name	Direction	Width	Function
O	Output	1-Bit	Buffer input
I	Input	1-Bit	Buffer output

Design Entry Method

This design element can be used in schematics.

In general, this element is inferred by the synthesis tool for any specified top-level input port to the design. It is generally not necessary to specify them in the source code however if desired, they be manually instantiated by either copying the instantiation code from the ISE Libraries Guide HDL Template and paste it into the top-level entity/module of your code. It is recommended to always put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level input port of the design and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Note Below	DEFAULT	Sets the programmable I/O standard for the input.
IBUF_DELAY_VALUE	Binary	0 thru 12	0	Specifies the amount of additional delay to add to the non-registered path out of the IOB
IFD_DELAY_VALUE	Binary	AUTO, 0 thru 6	AUTO	Specifies the amount of additional delay to add to the registered path within the IOB

Note Consult the device user guide or databook for the allowed values and the default value.

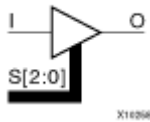
For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IBUF_DLY_ADJ

Primitive: Dynamically Adjustable Input Delay Buffer

IBUF_DLY_ADJ



Introduction

This design element is an input buffer with an adjustable delay element allowing dynamic delay adjustment (delay tuning) of an input signal into the FPGA. This is particularly useful for data aligning and capturing of high-speed input signals into the FPGA over process, voltage, and temperature variations. This component consists of a 3-bit select bus, which allows 8 unique values of delay to be added to the incoming signal. Additionally, the component can be programmed with a delay offset to delay adjustment within either the lower 8 or upper 8 of the 16 contiguous delay values.

See "For More Information" for details on the amount of delay and further details about usage of this component.

Port Descriptions

Name	Direction	Width	Function
O	Output	1-bit	Delayed output from the buffer
I	Input	1-bit	Differential input data (positive)
IB	Input	1-bit	Differential input data (negative)
S	Input	3-bit bus	Dynamic delay adjustment select lines

Design Entry Method

This design element can be used in schematics.

Available Attributes

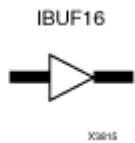
Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	Consult Data Sheet	"DEFAULT"	Specifies the I/O Standard to be used for this input.
DELAY_OFFSET	String	"OFF" or "ON"	"OFF"	When set to "OFF", the IBUFDS_DLY_ADJ operates at the lower range of delay values. This should be used when a smaller amount of additional delay is needed. When set to "ON", the component operates at the upper (longer) range of delay values. This should be used when a larger amount of additional delay is needed.
DIFF_TERM	Boolean	TRUE or FALSE	FALSE	Specifies the procedure for enabling or disabling (default) the internal differential termination capability.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IBUF16

Macro: 16-Bit Input Buffer



Introduction

Input Buffers isolate the internal circuit from the signals coming into the chip. This design element is contained in input/output blocks (IOBs) and allows the specification of the particular I/O Standard to configure the I/O. In general, an this element should be used for all single-ended data input or bidirectional pins.

Design Entry Method

This design element can be used in schematics.

In general, this element is inferred by the synthesis tool for any specified top-level input port to the design. It is generally not necessary to specify them in the source code however if desired, they be manually instantiated by either copying the instantiation code from the ISE Libraries Guide HDL Template and paste it into the top-level entity/module of your code. It is recommended to always put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level input port of the design and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Note Below	DEFAULT	Sets the programmable I/O standard for the input.
IBUF_DELAY_VALUE	Binary	0 thru 12	0	Specifies the amount of additional delay to add to the non-registered path out of the IOB
IFD_DELAY_VALUE	Binary	AUTO, 0 thru 6	AUTO	Specifies the amount of additional delay to add to the registered path within the IOB

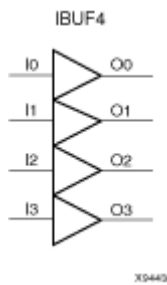
Note Consult the device user guide or databook for the allowed values and the default value.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IBUF4

Macro: 4-Bit Input Buffer



Introduction

Input Buffers isolate the internal circuit from the signals coming into the chip. This design element is contained in input/output blocks (IOBs) and allows the specification of the particular I/O Standard to configure the I/O. In general, an this element should be used for all single-ended data input or bidirectional pins.

Design Entry Method

This design element can be used in schematics.

In general, this element is inferred by the synthesis tool for any specified top-level input port to the design. It is generally not necessary to specify them in the source code however if desired, they be manually instantiated by either copying the instantiation code from the ISE Libraries Guide HDL Template and paste it into the top-level entity/module of your code. It is recommended to always put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level input port of the design and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Note Below	DEFAULT	Sets the programmable I/O standard for the input.
IBUF_DELAY_VALUE	Binary	0 thru 12	0	Specifies the amount of additional delay to add to the non-registered path out of the IOB
IFD_DELAY_VALUE	Binary	AUTO, 0 thru 6	AUTO	Specifies the amount of additional delay to add to the registered path within the IOB

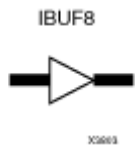
Note Consult the device user guide or databook for the allowed values and the default value.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IBUF8

Macro: 8-Bit Input Buffer



Introduction

Input Buffers isolate the internal circuit from the signals coming into the chip. This design element is contained in input/output blocks (IOBs) and allows the specification of the particular I/O Standard to configure the I/O. In general, an this element should be used for all single-ended data input or bidirectional pins.

Design Entry Method

This design element can be used in schematics.

In general, this element is inferred by the synthesis tool for any specified top-level input port to the design. It is generally not necessary to specify them in the source code however if desired, they be manually instantiated by either copying the instantiation code from the ISE Libraries Guide HDL Template and paste it into the top-level entity/module of your code. It is recommended to always put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level input port of the design and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Note Below	DEFAULT	Sets the programmable I/O standard for the input.
IBUF_DELAY_VALUE	Binary	0 thru 12	0	Specifies the amount of additional delay to add to the non-registered path out of the IOB
IFD_DELAY_VALUE	Binary	AUTO, 0 thru 6	AUTO	Specifies the amount of additional delay to add to the registered path within the IOB

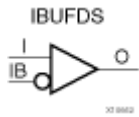
Note Consult the device user guide or databook for the allowed values and the default value.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IBUFDS

Primitive: Differential Signaling Input Buffer with Optional Delay



Introduction

This design element is an input buffer that supports low-voltage, differential signaling. In IBUFDS, a design level interface signal is represented as two distinct ports (I and IB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N). Optionally, a programmable differential termination feature is available to help improve signal integrity and reduce external components. Also available is a programmable delay to assist in the capturing of incoming data to the device.

Logic Table

Inputs		Outputs
I	IB	O
0	0	No Change
0	1	0
1	0	1
1	1	No Change

Port Descriptions

Name	Direction	Width	Function
O	Output	1-Bit	Diff_p Buffer input
IB	Input	1-Bit	Diff_n buffer input
I	Input	1-Bit	Buffer output

Design Entry Method

This design element can be used in schematics.

Put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level "master" input port of the design, the IB port to the top-level "slave" input port, and the O port to the logic in which this input is to source. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Note Below	DEFAULT	Sets the programmable I/O standard for the IOB
IBUF_DELAY_VALUE	Binary	0 thru 12	0	Specifies the amount of additional delay for the IOB
IFD_DELAY_VALUE	Binary	AUTO, 0 thru 6	AUTO	Specifies the amount of additional delay for the IOB
DIFF_TERM	Boolean	TRUE or FALSE	FALSE	Enables the built-in differential termination

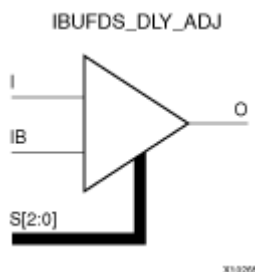
Note Consult the device user guide or databook for the allowed values and the default value.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IBUFDS_DLY_ADJ

Primitive: Dynamically Adjustable Differential Input Delay Buffer



Introduction

This design element is a differential input buffer with an adjustable delay element allowing dynamic delay adjustment (delay tuning) of an input signal into the FPGA. This is particularly useful for data aligning and capturing of high-speed input signals into the FPGA over process, voltage, and temperature variations. This component consists of a 3-bit select bus, which allows 8 unique values of delay to be added to the incoming signal. Additionally, the component can be programmed with a delay offset to delay adjustment within either the lower 8 or upper 8 of the 16 contiguous delay values.

Port Descriptions

Name	Direction	Width	Function
O	Output	1-bit	Delayed output from the buffer
I	Input	1-bit	Differential input data (positive)
IB	Input	1-bit	Differential input data (negative)
S	Input	3-bit bus	Dynamic delay adjustment select lines

Design Entry Method

Available Attributes

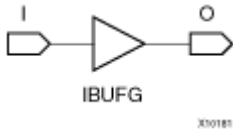
Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	Consult Data Sheet	"DEFAULT"	Specifies the I/O Standard to be used for this input.
DELAY_OFFSET	String	"OFF" or "ON"	"OFF"	When set to OFF, the IBUFDS_DLY_ADJ operates at the lower range of delay values. This should be used when a smaller amount of additional delay is needed. When set to ON, the component operates at the upper (longer) range of delay values. This should be used when a larger amount of additional delay is needed.
DIFF_TERM	Boolean	TRUE or FALSE	FALSE	Specifies the procedure for enabling or disabling internal differential termination capability.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IBUFG

Primitive: Dedicated Input Clock Buffer



Introduction

The IBUFG is a dedicated input to the device which should be used to connect incoming clocks to the FPGA to the global clock routing resources. The IBUFG provides dedicated connections to the DCM_SP and BUFG providing the minimum amount of clock delay and jitter to the device. The IBUFG input can only be driven by the global clock pins. The IBUFG output can drive CLKIN of a DCM_SP, BUFG, or your choice of logic. The IBUFG can be routed to your choice of logic to allow the use of the dedicated clock pins for general logic.

Port Descriptions

Name	Direction	Width	Function
O	Output	1-Bit	Clock Buffer input
I	Input	1-Bit	Clock Buffer output

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Note Below	"DEFAULT"	Sets the programmable I/O standard for the
IFD_DELAY_VALUE	Binary	AUTO, 0 thru 8	AUTO	Specifies the amount of additional delay to a within the IOB

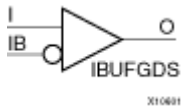
Note Consult the device user guide or databook for the allowed values and the default value.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IBUFGDS

Primitive: Differential Signaling Dedicated Input Clock Buffer and Optional Delay



Introduction

This design element is a dedicated differential signaling input buffer for connection to the clock buffer (BUFG) or DCM. In IBUFGDS, a design-level interface signal is represented as two distinct ports (I and IB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N). Optionally, a programmable differential termination feature is available to help improve signal integrity and reduce external components. Also available is a programmable delay to assist in the capturing of incoming data to the device.

Logic Table

Inputs		Outputs
I	IB	O
0	0	No Change
0	1	0
1	0	1
1	1	No Change

Port Descriptions

Name	Direction	Width	Function
O	Output	1-Bit	Diff_p Clock Buffer Input
IB	Input	1-Bit	Diff_n Clock Buffer Input
I	Input	1-Bit	Clock Buffer output

Design Entry Method

This design element can be used in schematics.

Put all I/O components on the top-level of the design to help facilitate hierarchical design methods. Connect the I port directly to the top-level "master" input port of the design, the IB port to the top-level "slave" input port and the O port to a DCM, BUFG or logic in which this input is to source. Some synthesis tools infer the BUFG automatically if necessary, when connecting an IBUFG to the clock resources of the FPGA. Specify the desired generic/defparam values in order to configure the proper behavior of the buffer.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
IOSTANDARD	String	See Note Below	"DEFAULT"	Sets the programmable I/O standard for the in
IFD_DELAY_VALUE	Binary	AUTO, 0 thru 6	AUTO	Specifies the amount of additional delay to ad registered path within the IOB.
DIFF_TERM	Boolean	TRUE or FALSE	FALSE	Enables the built-in differential termination re

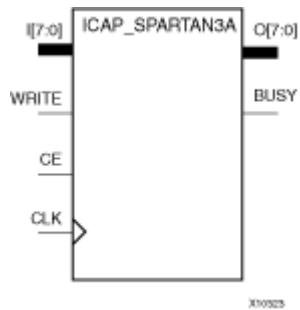
Note Consult the device user guide or databook for the allowed values and the default value.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ICAP_SPARTAN3A

Primitive: Internal Configuration Access Port



Introduction

This design element allows users access to the configuration functions of the FPGA from the FPGA fabric. This component's primary usage is to control Multiboot operations in Spartan-3A FPGAs. Using this component, commands and data can be written to and read from the configuration logic of the FPGA array. Because the improper use of this function can have a negative effect on the functionality and reliability of the FPGA, you are encouraged to gain a thorough understanding of this component before incorporating it into your designs.

Port Descriptions

Name	Direction	Width	Function
O	Output	8-bits	Configuration data output bus
Busy	Output	8-bits	Busy output
I	Input	8-bits	Configuration data input bus
WRITE	Input	8-bits	Active Low Write input
CE	Input8-bits	8-bits	Active Low Clock Enable Input
CLK	Input8-bits8-bits	8-bits	Clock Input

Design Entry Method

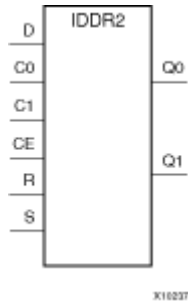
This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IDDR2

Primitive: Double Data Rate Input D Flip-Flop with Optional Data Alignment, Clock Enable and Programmable Synchronous or Asynchronous Set/Reset



Introduction

This design element is an input double data rate (DDR) register useful in capturing double data rate signals entering the FPGA. The IDDR2 requires two clocks to be connected to the component, C0 and C1, so that data is captured at the positive edge of both C0 and C1 clocks. The IDDR2 features an active high clock enable port, CE, which be used to suspend the operation of the registers, and both set and reset ports that be configured to be synchronous or asynchronous to the respective clocks. The IDDR2 has an optional alignment feature that allows both output data ports to the component to be aligned to a single clock.

Logic Table

Input						Output	
S	R	CE	D	C0	C1	Q0	Q1
1	x	x	x	x	x	INIT_Q0	INIT_Q1
0	1	x	x	x	x	not INIT_Q0	not INIT_Q1
0	0	0	x	x	x	No Change	No Change
0	0	1	D	Rising	x	D	No Change
0	0	1	D	x	Rising	No Change	D

Set/Reset can be synchronous via SRTYPE value

Design Entry Method

This design element can be used in schematics.

To change the default behavior of the IDDR2, modify attributes via the generic map (VHDL) or named parameter value assignment (Verilog) as a part of the instantiated component. The IDDR2 can be connected directly to a top-level input port in the design, where an appropriate input buffer can be inferred, or directly to an instantiated IBUF, IOBUF, IBUFDS or IOBUFDS. All inputs and outputs of this component should either be connected or properly tied off.

Available Attributes

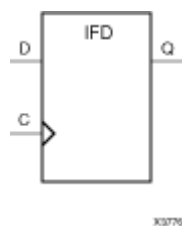
Attribute	Type	Allowed Values	Default	Description
DDR_ALIGNMENT	String	NONE, "C0" or "C1"	NONE"	Sets the output alignment more for the DDR reg available on the Q0 and Q1 outputs shortly after C1 positive clock edge. "C0" makes the data on positive edge of the C0 clock. "C1" makes the d to the positive edge of the C1 clock.
INIT_Q0	Integer	0 or 1	0	Sets initial state of the Q0 output to 0 or 1.
INIT_Q1	Integer	0 or 1	0	Sets initial state of the Q1 output to 0 or 1.
SRTYPE	String	"SYNC" or "ASYNC"	"SYNC"	Specifies SYNC" or "ASYNC" set/reset.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IFD

Macro: Input D Flip-Flop



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The (D) input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
D	C	Q
Dn	↑	Dn

Design Entry Method

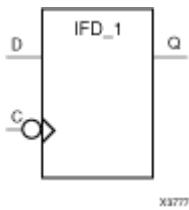
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IFD_1

Macro: Input D Flip-Flop with Inverted Clock (Asynchronous Preset)



Introduction

This design element is a D-type flip flop which is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input also provides data input for the flip-flop, which synchronizes data entering the chip. The D input data is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
D	C	Q
0	↓	0
1	↓	1

Design Entry Method

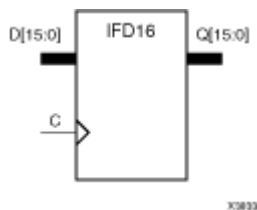
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IFD16

Macro: 16-Bit Input D Flip-Flop



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The (D) input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
D	C	Q
Dn	↑	Dn

Design Entry Method

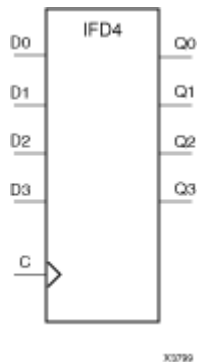
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IFD4

Macro: 4-Bit Input D Flip-Flop



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The (D) input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
D	C	Q
D _n	↑	D _n

Design Entry Method

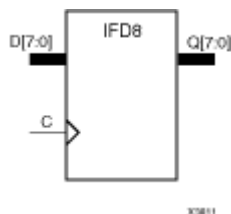
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IFD8

Macro: 8-Bit Input D Flip-Flop



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The (D) input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
D	C	Q
Dn	↑	Dn

Design Entry Method

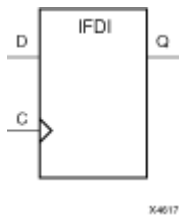
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IFDI

Macro: Input D Flip-Flop (Asynchronous Preset)



Introduction

This design element is a D-type flip-flop which is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input provides data input for the flip-flop, which synchronizes data entering the chip. The D input data is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
D	C	Q
D	↑	D

Design Entry Method

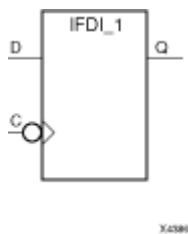
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IFDI_1

Macro: Input D Flip-Flop with Inverted Clock (Asynchronous Preset)



Introduction

The design element is a D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The (D) input provides data input for the flip-flop, which synchronizes data entering the chip. The data on input (D) is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
D	C	Q
0	↓	D

Design Entry Method

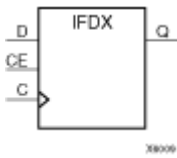
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IFDX

Macro: Input D Flip-Flop with Clock Enable



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The D input provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When CE is Low, flip-flop outputs do not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
CE	Dn	C	Qn
1	Dn	↑	Dn
0	X	X	No Change

Design Entry Method

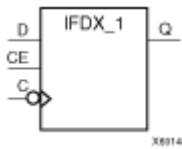
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IFDX_1

Macro: Input D Flip-Flop with Inverted Clock and Clock Enable



Introduction

This design element is a D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input also provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When the CE pin is Low, the output (Q) does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	D	↓	D
0	X	X	No Change

Design Entry Method

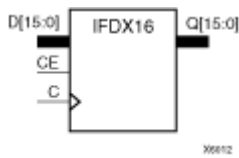
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IADX16

Macro: 16-Bit Input D Flip-Flops with Clock Enable



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The D input provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When CE is Low, flip-flop outputs do not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
CE	Dn	C	Qn
1	Dn	↑	Dn
0	X	X	No Change

Design Entry Method

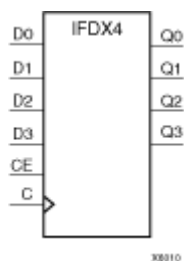
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IFDX4

Macro: 4-Bit Input D Flip-Flop with Clock Enable



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The D input provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When CE is Low, flip-flop outputs do not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
CE	Dn	C	Qn
1	Dn	↑	Dn
0	X	X	No Change

Design Entry Method

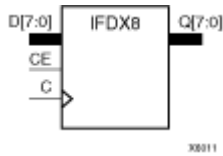
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IFDX8

Macro: 8-Bit Input D Flip-Flop with Clock Enable



Introduction

This D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD (without using an IBUF). The D input provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When CE is Low, flip-flop outputs do not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
CE	Dn	C	Qn
1	Dn	↑	Dn
0	X	X	No Change

Design Entry Method

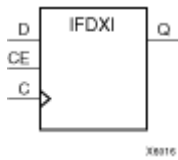
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IFDXI

Macro: Input D Flip-Flop with Clock Enable (Asynchronous Preset)



Introduction

The design element is a D-type flip-flop is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The D input provides data input for the flip-flop, which synchronizes data entering the chip. When CE is High, the data on input D is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When the CE pin is Low, the output (Q) does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	D	↑	D
0	X	X	No Change

Design Entry Method

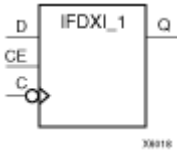
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IFDXI_1

Macro: Input D Flip-Flop with Inverted Clock and Clock Enable (Asynchronous Preset)



Introduction

The design element is a D-type flip-flop that is contained in an input/output block (IOB). The input (D) of the flip-flop is connected to an IPAD or an IOPAD. The (D) input provides data input for the flip-flop, which synchronizes data entering the chip. When (CE) is High, the data on input (D) is loaded into the flip-flop during the High-to-Low clock (C) transition and appears at the output (Q). The clock input can be driven by internal logic or through another external pin. When the (CE) pin is Low, the output (Q) does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	D	↓	D
0	X	X	No Change

Design Entry Method

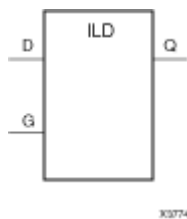
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ILD

Macro: Transparent Input Data Latch



Introduction

This design element is a single, transparent data latch that holds transient data entering a chip. This latch is contained in an input/output block (IOB). The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (G) is High, data on the input (D) appears on the output (Q). Data on the D input during the High-to-Low G transition is stored in the latch.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Output
G	D	Q
1	D	D
0	X	No Change
∅	D	D

Design Entry Method

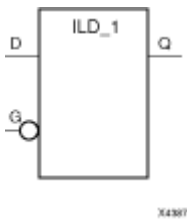
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ILD_1

Macro: Transparent Input Data Latch with Inverted Gate



Introduction

This design element is a transparent data latch that holds transient data entering a chip. When the gate input (G) is Low, data on the data input (D) appears on the data output (Q). Data on (D) during the Low-to-High (G) transition is stored in the latch.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
G	D	Q
0	D	D
1	X	D
↑	D	D

Design Entry Method

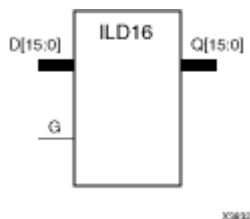
This component is inside the IOB. It cannot be directly inferred. The most common design practice is to infer a regular component and put an IOB=TRUE attribute on the component in the UCF file or in the code. For instance, to get an ILD_1, you would infer an ILD_1 and put the IOB = TRUE attribute on the component. Or, you could use the map option `-pri 0` to pack all input registers into the IOBs.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ILD16

Macro: Transparent Input Data Latch



Introduction

These design elements are multiple transparent data latches that hold transient data entering a chip. The ILD latch is contained in an input/output block (IOB). The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (G) is High, data on the inputs (D) appears on the outputs (Q). Data on the D inputs during the High-to-Low G transition is stored in the latch.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
G	D	Q
1	D	D
0	X	No Change
↓	D	D

Design Entry Method

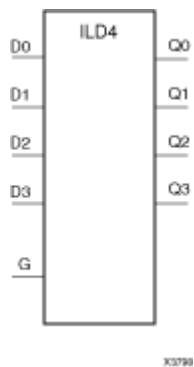
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ILD4

Macro: Transparent Input Data Latch



Introduction

These design elements are multiple transparent data latches that hold transient data entering a chip. The ILD latch is contained in an input/output block (IOB). The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (G) is High, data on the inputs (D) appears on the outputs (Q). Data on the D inputs during the High-to-Low G transition is stored in the latch.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
G	D	Q
1	D	D
0	X	No Change
↓	D	D

Design Entry Method

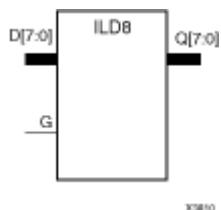
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ILD8

Macro: Transparent Input Data Latch



Introduction

These design elements are multiple transparent data latches that hold transient data entering a chip. The ILD latch is contained in an input/output block (IOB). The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF). When the gate input (G) is High, data on the inputs (D) appears on the outputs (Q). Data on the D inputs during the High-to-Low G transition is stored in the latch.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
G	D	Q
1	D	D
0	X	No Change
↓	D	D

Design Entry Method

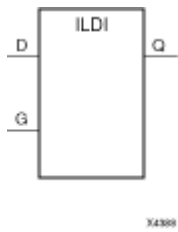
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ILDI

Macro: Transparent Input Data Latch (Asynchronous Preset)



Introduction

This design element is a transparent data latch that holds transient data entering a chip. When the gate input (G) is High, data on the input (D) appears on the output (Q). Data on the D input during the High-to-Low G transition is stored in the latch.

The ILDI is the input flip-flop master latch. It is possible to access two different outputs from the input flip-flop: one that responds to the level of the clock signal and another that responds to an edge of the clock signal. When using both outputs from the same input flip-flop, a transparent High latch (ILDI) corresponds to a falling edge-triggered flip-flop (IFDI_1). Similarly, a transparent Low latch (ILDI_1) corresponds to a rising edge-triggered flip-flop (IFDI).

The latch is asynchronously preset, output High, when power is applied.

For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
G	D	Q
1	D	D
0	X	D
↓	D	D

Design Entry Method

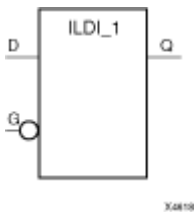
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ILDI_1

Macro: Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)



Introduction

This design element is a transparent data latch that holds transient data entering a chip. When the gate input (G) is Low, data on the data input (D) appears on the data output (Q). Data on D during the Low-to-High G transition is stored in the latch.

The latch is asynchronously preset, output High, when power is applied.

For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
G	D	Q
0	1	1
0	0	0
1	X	D
↑	D	D

Design Entry Method

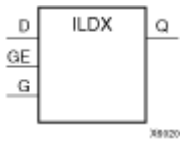
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ILDX

Macro: Transparent Input Data Latch



Introduction

This design element is single or multiple transparent data latches that holds transient data entering a chip. The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF).

The ILDX is the input flip-flop master latch. Two outputs can be accessed from the input flip-flop: one that responds to the level of the clock signal and another that responds to an edge of the clock signal. When using both outputs from the same input flip-flop, a transparent High latch (ILDX) corresponds to a falling edge-triggered flip-flop (IFDX_1). Similarly, a transparent Low latch (ILDX_1) corresponds to a rising edge-triggered flip-flop (IFDX).

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
GE	G	D	Q
0	X	X	No Change
1	0	X	No Change
1	1	D	D

Design Entry Method

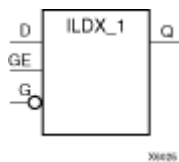
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ILDX_1

Macro: Transparent Input Data Latch with Inverted Gate



Introduction

This design element is a transparent data latch that holds transient data entering a chip. When the gate input (G) is Low, data on the data input (D) appears on the data output (Q). Data on D during the Low-to-High G transition is stored in the latch.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
GE	G	D	Q
0	X	X	No Change
1	1	X	No Change
1	0	1	1
1	0	0	0
1	↑	D	D

Design Entry Method

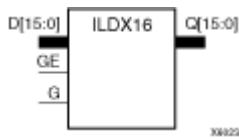
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ILDX16

Macro: Transparent Input Data Latch



Introduction

This design element is single or multiple transparent data latches that holds transient data entering a chip. The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF).

The ILDX is the input flip-flop master latch. Two outputs can be accessed from the input flip-flop: one that responds to the level of the clock signal and another that responds to an edge of the clock signal. When using both outputs from the same input flip-flop, a transparent High latch (ILDX) corresponds to a falling edge-triggered flip-flop (IFDX_1). Similarly, a transparent Low latch (ILDX_1) corresponds to a rising edge-triggered flip-flop (IFDX)

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
GE	G	D	Q
0	X	X	No Change
1	0	X	No Change
1	1	D	D

Design Entry Method

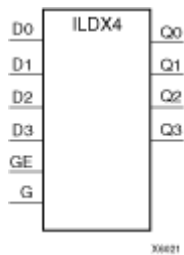
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ILDX4

Macro: Transparent Input Data Latch



Introduction

This design element is single or multiple transparent data latches that holds transient data entering a chip. The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF).

The ILDX is the input flip-flop master latch. Two outputs can be accessed from the input flip-flop: one that responds to the level of the clock signal and another that responds to an edge of the clock signal. When using both outputs from the same input flip-flop, a transparent High latch (ILDX) corresponds to a falling edge-triggered flip-flop (IFDX_1). Similarly, a transparent Low latch (ILDX_1) corresponds to a rising edge-triggered flip-flop (IFDX).

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs			Outputs
GE	G	D	Q
0	X	X	No Change
1	0	X	No Change
1	1	D	D

Design Entry Method

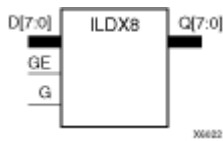
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ILDX8

Macro: Transparent Input Data Latch



Introduction

This design element is single or multiple transparent data latches that holds transient data entering a chip. The latch input (D) is connected to an IPAD or an IOPAD (without using an IBUF).

The ILDX is the input flip-flop master latch. Two outputs can be accessed from the input flip-flop: one that responds to the level of the clock signal and another that responds to an edge of the clock signal. When using both outputs from the same input flip-flop, a transparent High latch (ILDX) corresponds to a falling edge-triggered flip-flop (IFDX_1). Similarly, a transparent Low latch (ILDX_1) corresponds to a rising edge-triggered flip-flop (IFDX).

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
GE	G	D	Q
0	X	X	No Change
1	0	X	No Change
1	1	D	D

Design Entry Method

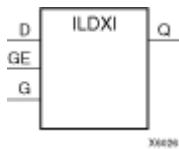
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ILDXI

Macro: Transparent Input Data Latch (Asynchronous Preset)



Introduction

This design element is a transparent data latch that holds transient data entering a chip. When the gate input (G) is High, data on the input (D) appears on the output (Q). Data on the (D) input during the High-to-Low (G) transition is stored in the latch.

The ILDXI is the input flip-flop master latch. Two outputs can be accessed from the input flip-flop: one that responds to the level of the clock signal and another that responds to an edge of the clock signal. When using both outputs from the same input flip-flop, a transparent High latch (ILDXI) corresponds to a falling edge-triggered flip-flop (IFDXI_1). Similarly, a transparent Low latch (ILDXI_1) corresponds to a rising edge-triggered flip-flop (IFDXI).

The latch is asynchronously preset, output High, when power is applied.

For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
GE	G	D	Q
0	X	X	No Change
1	0	X	No Change
1	1	D	D
1	↓	D	D

Design Entry Method

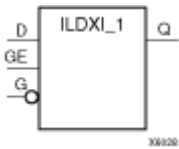
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ILDXI_1

Macro: Transparent Input Data Latch with Inverted Gate (Asynchronous Preset)



Introduction

This design element is a transparent data latch that holds transient data entering a chip.

The latch is asynchronously preset, output High, when power is applied.

For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
GE	G	D	Q
0	X	X	No Change
1	1	X	No Change
1	0	D	D
1	↑	D	D

Design Entry Method

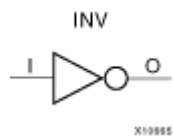
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

INV

Primitive: Inverter



Introduction

This design element is a single inverter that identifies signal inversions in a schematic.

Design Entry Method

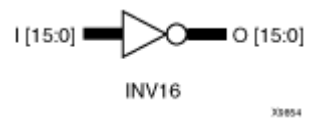
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

INV16

Macro: 16 Inverters



Introduction

This design element is a multiple inverter that identifies signal inversions in a schematic.

Design Entry Method

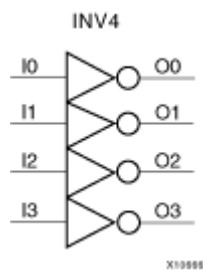
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

INV4

Macro: Four Inverters



Introduction

This design element is a multiple inverter that identifies signal inversions in a schematic.

Design Entry Method

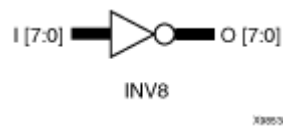
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

INV8

Macro: Eight Inverters



Introduction

This design element is a multiple inverter that identifies signal inversions in a schematic.

Design Entry Method

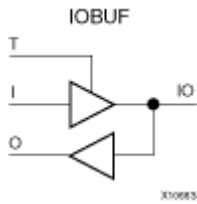
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IOBUF

Primitive: Bi-Directional Buffer



Introduction

The design element is a bidirectional single-ended I/O Buffer used to connect internal logic to an external bidirectional pin.

Logic Table

Inputs		Bidirectional	Outputs
T	I	IO	O
1	X	Z	X
0	1	1	1
0	0	0	0

Port Descriptions

Name	Direction	Width	Function
O	Output	1-Bit	Buffer output
IO	Inout	1-Bit	Buffer inout
I	Input	1-Bit	Buffer input
T	Input	1-Bit	3-State enable input

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Descriptions
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Selects output drive strength (mA) for the SelectIO buffers that use the LVTTTL, LVCMOS12, LVCMOS15, LVCMOS18, LVCMOS25, or LVCMOS33 interface I/O standard.
IOSTANDARD	String	"DEFAULT"	"DEFAULT"	Use to assign an I/O standard to an I/O primitive.
IBUF_DELAY_VALUE	Binary	0 thru 12	0	Specifies the amount of additional delay to add to the non-registered path out of the IOB

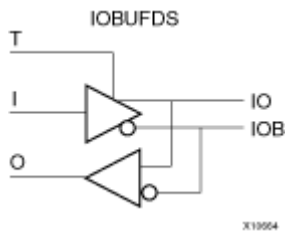
Attribute	Type	Allowed Values	Default	Descriptions
IFD_DELAY_VALUE	Binary	AUTO, 0 thru 6	AUTO	Specifies the amount of additional delay to add to the registered path within the IOB
SLEW	Integer	"SLOW", "FAST"	"SLOW"	Sets the output rise and fall time.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

IOBUFDS

Primitive: 3-State Differential Signaling I/O Buffer with Active Low Output Enable



Introduction

The design element is a bidirectional buffer that supports low-voltage, differential signaling. For the IOBUFDS, a design level interface signal is represented as two distinct ports (IO and IOB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N). Optionally, a programmable differential termination feature is available to help improve signal integrity and reduce external components. Also available is a programmable delay to assist in the capturing of incoming data to the device.

Logic Table

Inputs		Bidirectional		Outputs
I	T	IO	IOB	O
X	1	Z	Z	No Change
0	0	0	1	0
1	0	1	0	1

Port Descriptions

Name	Direction	Width	Function
O	Output	1-Bit	Buffer output
IO	Inout	1-Bit	Diff_p inout
IOB	Inout	1-Bit	Diff_n inout
I	Input	1-Bit	Buffer input
T	Input	1-Bit	3-state enable input

Design Entry Method

This design element can be used in schematics.

Available Attributes

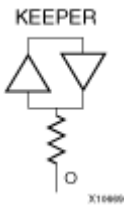
Attribute	Type	Allowed Values	Default	Descriptions
IFD_DELAY_VALUE	String	"AUTO" or 0 to 6	"AUTO"	Specifies the amount of additional delay to add to the registered path within the IOB.
IOSTANDARD	String	"DEFAULT"	"DEFAULT"	Use to assign an I/O standard to an I/O primitive.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

KEEPER

Primitive: KEEPER Symbol



Introduction

The design element is a weak keeper element that retains the value of the net connected to its bidirectional O pin. For example, if a logic 1 is being driven onto the net, KEEPER drives a weak/resistive 1 onto the net. If the net driver is then 3-stated, KEEPER continues to drive a weak/resistive 1 onto the net.

Port Descriptions

Name	Direction	Width	Function
O	Output	1-Bit	Keeper output

Design Entry Method

This design element can be used in schematics.

This element can be connected to a net in the following locations on a top-level schematic file:

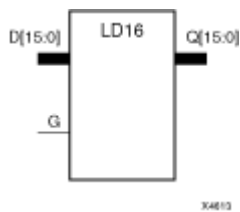
- A net connected to an input IO Marker
- A net connected to both an output IO Marker and 3-statable IO element, such as an OBUFT.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

LD16

Macro: Multiple Transparent Data Latch



Introduction

This design element has 16 transparent data latches with a common gate enable (G). The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
G	D	Q
1	D	D
0	X	No Change
↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

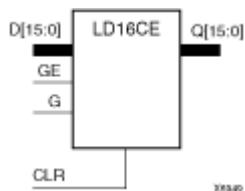
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 16-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

LD16CE

Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable



Introduction

This design element has 16 transparent data latches with asynchronous clear and gate enable. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) outputs Low. (Q) reflects the data (D) inputs while the gate (G) and gate enable (GE) are High, and (CLR) is Low. If (GE) is Low, data on (D) cannot be latched. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs				Outputs
CLR	GE	G	Dn	Qn
1	X	X	X	0
0	0	X	X	No Change
0	1	1	Dn	Dn
0	1	0	X	No Change
0	1	↓	Dn	Dn

Dn = referenced input, for example, D0, D1, D2
 Qn = referenced output, for example, Q0, Q1, Q2

Design Entry Method

This design element is only for use in schematics.

Available Attributes

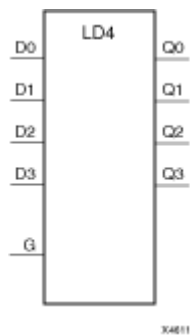
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 16-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

LD4

Macro: Multiple Transparent Data Latch



Introduction

This design element has four transparent data latches with a common gate enable (G). The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
G	D	Q
1	D	D
0	X	No Change
↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

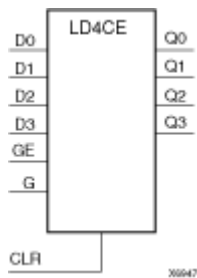
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 4-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

LD4CE

Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable



Introduction

This design element has 4 transparent data latches with asynchronous clear and gate enable. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) outputs Low. (Q) reflects the data (D) inputs while the gate (G) and gate enable (GE) are High, and (CLR) is Low. If (GE) is Low, data on (D) cannot be latched. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
CLR	GE	G	Dn	Qn
1	X	X	X	0
0	0	X	X	No Change
0	1	1	Dn	Dn
0	1	0	X	No Change
0	1	↓	Dn	Dn

Dn = referenced input, for example, D0, D1, D2
 Qn = referenced output, for example, Q0, Q1, Q2

Design Entry Method

This design element is only for use in schematics.

Available Attributes

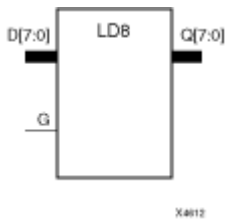
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 4-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

LD8

Macro: Multiple Transparent Data Latch



Introduction

This design element has 8 transparent data latches with a common gate enable (G). The data output (Q) of the latch reflects the data (D) input while the gate enable (G) input is High. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
G	D	Q
1	D	D
0	X	No Change
↓	Dn	Dn

Design Entry Method

This design element is only for use in schematics.

Available Attributes

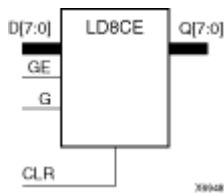
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 8-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

LD8CE

Macro: Transparent Data Latch with Asynchronous Clear and Gate Enable



Introduction

This design element has 8 transparent data latches with asynchronous clear and gate enable. When the asynchronous clear input (CLR) is High, it overrides the other inputs and resets the data (Q) outputs Low. (Q) reflects the data (D) inputs while the gate (G) and gate enable (GE) are High, and (CLR) is Low. If (GE) is Low, data on (D) cannot be latched. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) or (GE) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
CLR	GE	G	Dn	Qn
1	X	X	X	0
0	0	X	X	No Change
0	1	1	Dn	Dn
0	1	0	X	No Change
0	1	↓	Dn	Dn

Dn = referenced input, for example, D0, D1, D2
 Qn = referenced output, for example, Q0, Q1, Q2

Design Entry Method

This design element is only for use in schematics.

Available Attributes

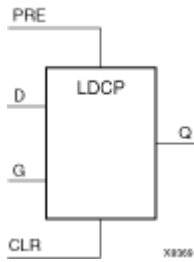
Attribute	Type	Allowed Values	Default	Description
INIT	Binary	Any 8-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

LDCP

Primitive: Transparent Data Latch with Asynchronous Clear and Preset



Introduction

The design element is a transparent data latch with data (D), asynchronous clear (CLR) and preset (PRE) inputs. When (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. When PRE is High and (CLR) is low, it presets the data (Q) output High. (Q) reflects the data (D) input while the gate (G) input is High and (CLR) and PRE are Low. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
CLR	PRE	G	D	Q
1	X	X	X	0
0	1	X	X	1
0	0	1	D	D
0	0	0	X	No Change
0	0	↓	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

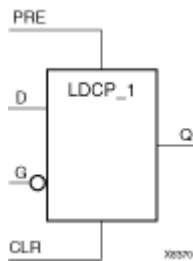
Attribute	Type	Allowed Values	Default	Description
INIT	INTEGER	0 or 1	0	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

LDCP_1

Primitive: Transparent Data Latch with Asynchronous Clear and Preset and Inverted Gate



Introduction

This design element is a transparent data latch with data (D), asynchronous clear (CLR), preset (PRE) inputs, and inverted gate (G). When (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. When (PRE) is High and (CLR) is Low, it presets the data (Q) output High. (Q) reflects the data (D) input while gate (G) input, (CLR), and (PRE) are Low. The data on the (D) input during the Low-to-High gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) remains High.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs
CLR	PRE	G	D	Q
1	X	X	X	0
0	1	X	X	1
0	0	0	D	D
0	0	1	X	No Change
0	0	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

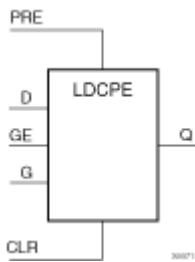
Attribute	Type	Allowed Values	Default	Description
INIT	Integer	0 or 1	0	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

LDCPE

Primitive: Transparent Data Latch with Asynchronous Clear and Preset and Gate Enable



Introduction

This design element is a transparent data latch with data (D), asynchronous clear (CLR), asynchronous preset (PRE), and gate enable (GE). When (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. When (PRE) is High and (CLR) is Low, it presets the data (Q) output High. Q reflects the data (D) input while the gate (G) input and gate enable (GE) are High and (CLR) and PRE are Low. The data on the (D) input during the High-to-Low gate transition is stored in the latch. The data on the Q output remains unchanged as long as (G) or (GE) remains Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs					Outputs
CLR	PRE	GE	G	D	Q
1	X	X	X	X	0
0	1	X	X	X	1
0	0	0	X	X	No Change
0	0	1	1	0	0
0	0	1	1	1	1
0	0	1	0	X	No Change
0	0	1	↓	D	D

Port Descriptions

Name	Direction	Width	Function
Q	Output	1-Bit	Data Output
CLR	Input	1-Bit	Asynchronous clear/reset input
D	Input	1-Bit	Data Input
G	Input	1-Bit	Gate Input
GE	Input	1-Bit	Gate Enable Input
PRE	Input	1-Bit	Asynchronous preset/set input

Design Entry Method

This design element can be used in schematics.

Available Attributes

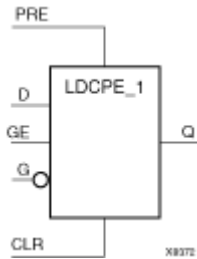
Attribute	Type	Allowed Values	Default	Description
INIT	Integer	0 or 1	0	Sets the initial value of Q output after configuration

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

LDCPE_1

Primitive: Transparent Data Latch with Asynchronous Clear and Preset, Gate Enable, and Inverted Gate



Introduction

This design element is a transparent data latch with data (D), asynchronous clear (CLR), asynchronous preset (PRE), gate enable (GE), and inverted gate (G). When (CLR) is High, it overrides the other inputs and resets the data (Q) output Low. When PRE is High and (CLR) is Low, it presets the data (Q) output High. (Q) reflects the data (D) input while gate enable (GE) is High and gate (G), (CLR), and (PRE) are Low. The data on the (D) input during the Low-to-High gate transition is stored in the latch. The data on the (Q) output remains unchanged as long as (G) is High or (GE) is Low.

This latch is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs					Outputs
CLR	PRE	GE	G	D	Q
1	X	X	X	X	0
0	1	X	X	X	1
0	0	0	X	X	No Change
0	0	1	0	D	D
0	0	1	1	X	No Change
0	0	1	↑	D	D

Design Entry Method

This design element is only for use in schematics.

Available Attributes

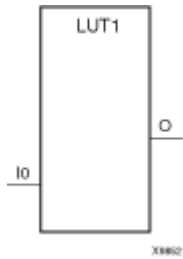
Attribute	Type	Allowed Values	Default	Description
INIT	Integer	0 or 1	0	Specifies the initial value upon power-up or the assertion of GSR for the (Q) port.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

LUT1

Primitive: 1-Bit Look-Up-Table with General Output



Introduction

This design element is a 1-bit look-up-tables (LUT) with general output (O).

An INIT attribute with an appropriate number of hexadecimal digits for the number of inputs must be attached to the LUT to specify its function. This element provides a look-up-table version of a buffer or inverter. These elements are the basic building blocks. Two LUTs are available in each CLB slice; four LUTs are available in each CLB. Multiple variants of LUTs accommodate additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Truth Table Method -A common method to determine the desired INIT value for a LUT is using a truth table. To do so, simply create a binary truth table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and more self-documenting than the above method however does require the code to first specify the appropriate parameters.

Logic Table

Inputs	Outputs
I0	O
0	INIT[0]
1	INIT[1]
INIT = Binary number assigned to the INIT attribute	

Design Entry Method

This design element can be used in schematics.

Available Attributes

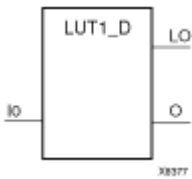
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 2-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

LUT1_D

Primitive: 1-Bit Look-Up-Table with Dual Output



Introduction

This design element is a 1-bit look-up-table (LUT) with two functionally identical outputs, O and LO. *LUTD_1* provides a look-up-table version of a buffer or inverter.

The O output is a general interconnect. The LO output is used to connect to another output within the same CLB slice and to the fast connect buffer. A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Truth Table Method -A common method to determine the desired INIT value for a LUT is using a truth table. To do so, simply create a binary truth table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and more self-documenting than the above method however does require the code to first specify the appropriate parameters.

Logic Table

Inputs	Outputs	
I0	O	LO
0	INIT[0]	INIT[0]
1	INIT[1]	INIT[1]
INIT = Binary number assigned to the INIT attribute		

Design Entry Method

This design element can be used in schematics.

Available Attributes

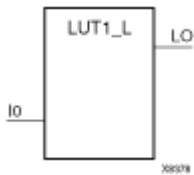
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 2-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

LUT1_L

Primitive: 1-Bit Look-Up-Table with Local Output



Introduction

This design element is a 1-bit look-up-tables (LUTs) with a local output (LO) that is used to connect to another output within the same CLB slice and to the fast connect buffer. It provides a look-up-table version of a buffer or inverter.

A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Truth Table Method -A common method to determine the desired INIT value for a LUT is using a truth table. To do so, simply create a binary truth table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and more self-documenting than the above method however does require the code to first specify the appropriate parameters.

Logic Table

Inputs	Outputs
I0	LO
0	INIT[0]
1	INIT[1]
INIT = Binary number assigned to the INIT attribute	

Design Entry Method

This design element can be used in schematics.

Available Attributes

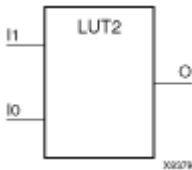
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 2-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

LUT2

Primitive: 2-Bit Look-Up-Table with General Output



Introduction

This design element is a 2-bit look-up-table (LUT) with general output (O).

An INIT attribute with an appropriate number of hexadecimal digits for the number of inputs must be attached to the LUT to specify its function. This element provides a look-up-table version of a buffer or inverter. These elements are the basic building blocks. Two LUTs are available in each CLB slice; four LUTs are available in each CLB. Multiple variants of LUTs accommodate additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Truth Table Method -A common method to determine the desired INIT value for a LUT is using a truth table. To do so, simply create a binary truth table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and more self-documenting than the above method however does require the code to first specify the appropriate parameters.

Logic Table

Inputs		Outputs
I1	I0	O
0	0	INIT[0]
0	1	INIT[1]
1	0	INIT[2]
1	1	INIT[3]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute		

Design Entry Method

This design element can be used in schematics.

Available Attributes

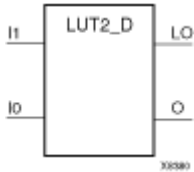
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 4-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

LUT2_D

Primitive: 2-Bit Look-Up-Table with Dual Output



Introduction

This design element is a 2-bit look-up-tables (LUTs) with two functionally identical outputs, O and LO.

The O output is a general interconnect. The LO output is used to connect to another output within the same CLB slice and to the fast connect buffer. A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Truth Table Method -A common method to determine the desired INIT value for a LUT is using a truth table. To do so, simply create a binary truth table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and more self-documenting that the above method however does require the code to first specify the appropriate parameters.

Logic Table

Inputs		Outputs	
I1	I0	O	LO
0	0	INIT[0]	INIT[0]
0	1	INIT[1]	INIT[1]
1	0	INIT[2]	INIT[2]
1	1	INIT[3]	INIT[3]

INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute

Design Entry Method

This design element can be used in schematics.

Available Attributes

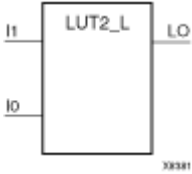
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 4-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

LUT2_L

Primitive: 2-Bit Look-Up-Table with Local Output



Introduction

This design element is a 2-bit look-up-tables (LUTs) with a local output (LO) that is used to connect to another output within the same CLB slice and to the fast connect buffer. It provides a look-up-table version of a buffer or inverter.

A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Truth Table Method -A common method to determine the desired INIT value for a LUT is using a truth table. To do so, simply create a binary truth table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and more self-documenting than the above method however does require the code to first specify the appropriate parameters.

Logic Table

Inputs		Outputs
I1	I0	LO
0	0	INIT[0]
0	1	INIT[1]
1	0	INIT[2]
1	1	INIT[3]
INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute		

Design Entry Method

This design element can be used in schematics.

Available Attributes

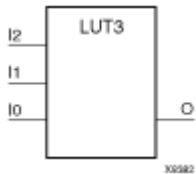
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 4-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

LUT3

Primitive: 3-Bit Look-Up-Table with General Output



Introduction

This design element is a 3-bit look-up-table (LUT) with general output (O). A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

An INIT attribute with an appropriate number of hexadecimal digits for the number of inputs must be attached to the LUT to specify its function. This element provides a look-up-table version of a buffer or inverter. These elements are the basic building blocks. Two LUTs are available in each CLB slice; four LUTs are available in each CLB. Multiple variants of LUTs accommodate additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

Logic Table

Inputs			Outputs
I2	I1	I0	O
0	0	0	INIT[0]
0	0	1	INIT[1]
0	1	0	INIT[2]
0	1	1	INIT[3]
1	0	0	INIT[4]
1	0	1	INIT[5]
1	1	0	INIT[6]
1	1	1	INIT[7]

INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute

Design Entry Method

This design element can be used in schematics.

Available Attributes

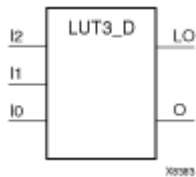
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 8-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

LUT3_D

Primitive: 3-Bit Look-Up-Table with Dual Output



Introduction

This design element is a 3-bit look-up-tables (LUTs) with two functionally identical outputs, O and LO.

The O output is a general interconnect. The LO output is used to connect to another output within the same CLB slice and to the fast connect buffer. A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Logic Table Method -A common method to determine the desired INIT value for a LUT is using a truth table. To do so, simply create a binary logic table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and more self-documenting than the above method however does require the code to first specify the appropriate parameters.

Logic Table

Inputs			Outputs	
I2	I1	I0	O	LO
0	0	0	INIT[0]	INIT[0]
0	0	1	INIT[1]	INIT[1]
0	1	0	INIT[2]	INIT[2]
0	1	1	INIT[3]	INIT[3]
1	0	0	INIT[4]	INIT[4]
1	0	1	INIT[5]	INIT[5]
1	1	0	INIT[6]	INIT[6]
1	1	1	INIT[7]	INIT[7]

INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute

Design Entry Method

This design element can be used in schematics.

Available Attributes

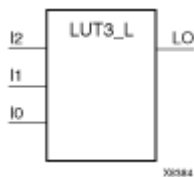
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 8-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

LUT3_L

Primitive: 3-Bit Look-Up-Table with Local Output



Introduction

This design element is a 3-bit look-up-tables (LUTs) with a local output (LO) that is used to connect to another output within the same CLB slice and to the fast connect buffer. It provides a look-up-table version of a buffer or inverter.

A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Truth Table Method -A common method to determine the desired INIT value for a LUT is using a truth table. To do so, simply create a binary truth table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and more self-documenting than the above method however does require the code to first specify the appropriate parameters.

Logic Table

Inputs			Outputs
I2	I1	I0	LO
0	0	0	INIT[0]
0	0	1	INIT[1]
0	1	0	INIT[2]
0	1	1	INIT[3]
1	0	0	INIT[4]
1	0	1	INIT[5]
1	1	0	INIT[6]
1	1	1	INIT[7]

INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute

Design Entry Method

This design element can be used in schematics.

Available Attributes

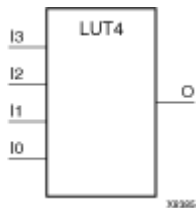
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 8-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

LUT4

Primitive: 4-Bit Look-Up-Table with General Output



Introduction

This design element is a 4-bit look-up-tables (LUT) with general output (O).

An INIT attribute with an appropriate number of hexadecimal digits for the number of inputs must be attached to the LUT to specify its function. This element provides a look-up-table version of a buffer or inverter. These elements are the basic building blocks. Two LUTs are available in each CLB slice; four LUTs are available in each CLB. Multiple variants of LUTs accommodate additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Truth Table Method -A common method to determine the desired INIT value for a LUT is using a truth table. To do so, simply create a binary truth table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and more self-documenting that the above method however does require the code to first specify the appropriate parameters.

Logic Table

Inputs				Outputs
I3	I2	I1	I0	O
0	0	0	0	INIT[0]
0	0	0	1	INIT[1]
0	0	1	0	INIT[2]
0	0	1	1	INIT[3]
0	1	0	0	INIT[4]
0	1	0	1	INIT[5]
0	1	1	0	INIT[6]
0	1	1	1	INIT[7]
1	0	0	0	INIT[8]
1	0	0	1	INIT[9]
1	0	1	0	INIT[10]
1	0	1	1	INIT[11]
1	1	0	0	INIT[12]

Inputs				Outputs
I3	I2	I1	I0	O
1	1	0	1	INIT[13]
1	1	1	0	INIT[14]
1	1	1	1	INIT[15]

INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute

Design Entry Method

This design element can be used in schematics.

Available Attributes

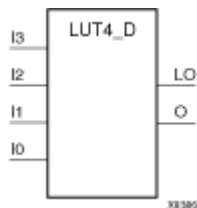
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

LUT4_D

Primitive: 4-Bit Look-Up-Table with Dual Output



Introduction

This design element is a 4-bit look-up-tables (LUTs) with two functionally identical outputs, O and LO

The O output is a general interconnect. The LO output is used to connect to another output within the same CLB slice and to the fast connect buffer. A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Truth Table Method -A common method to determine the desired INIT value for a LUT is using a truth table. To do so, simply create a binary truth table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and more self-documenting than the above method however does require the code to first specify the appropriate parameters.

Logic Table

Inputs				Outputs	
I3	I2	I1	I0	O	LO
0	0	0	0	INIT[0]	INIT[0]
0	0	0	1	INIT[1]	INIT[1]
0	0	1	0	INIT[2]	INIT[2]
0	0	1	1	INIT[3]	INIT[3]
0	1	0	0	INIT[4]	INIT[4]
0	1	0	1	INIT[5]	INIT[5]
0	1	1	0	INIT[6]	INIT[6]
0	1	1	1	INIT[7]	INIT[7]
1	0	0	0	INIT[8]	INIT[8]
1	0	0	1	INIT[9]	INIT[9]
1	0	1	0	INIT[10]	INIT[10]
1	0	1	1	INIT[11]	INIT[11]
1	1	0	0	INIT[12]	INIT[12]
1	1	0	1	INIT[13]	INIT[13]

Inputs				Outputs	
I3	I2	I1	I0	O	LO
1	1	1	0	INIT14]	INIT14]
1	1	1	1	INIT[15]	INIT[15]

INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute

Design Entry Method

This design element can be used in schematics.

Available Attributes

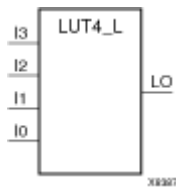
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

LUT4_L

Primitive: 4-Bit Look-Up-Table with Local Output



Introduction

This design element is a 4-bit look-up-tables (LUTs) with a local output (LO) that is used to connect to another output within the same CLB slice and to the fast connect buffer. It provides a look-up-table version of a buffer or inverter.

A mandatory INIT attribute, with an appropriate number of hexadecimal digits for the number of inputs, must be attached to the LUT to specify its function.

The INIT parameter for the FPGA LUT primitive is what gives the LUT its logical value. By default, this value is zero, thus driving the output to a zero regardless of the input values (acting as a ground). However, in most cases a new INIT value must be determined in order to specify the logic function for the LUT primitive. There are at least two methods by which the LUT value can be determined:

The Truth Table Method -A common method to determine the desired INIT value for a LUT is using a truth table. To do so, simply create a binary truth table of all possible inputs, specify the desired logic value of the output and then create the INIT string from those output values.

The Equation Method -Another method to determine the LUT value is to define parameters for each input to the LUT that correspond to their listed truth value and use those to build the logic equation you are after. This method is easier to understand once you have grasped the concept and more self-documenting than the above method however does require the code to first specify the appropriate parameters.

Logic Table

Inputs				Outputs
I3	I2	I1	I0	LO
0	0	0	0	INIT[0]
0	0	0	1	INIT[1]
0	0	1	0	INIT[2]
0	0	1	1	INIT[3]
0	1	0	0	INIT[4]
0	1	0	1	INIT[5]
0	1	1	0	INIT[6]
0	1	1	1	INIT[7]
1	0	0	0	INIT[8]
1	0	0	1	INIT[9]
1	0	1	0	INIT[10]
1	0	1	1	INIT[11]
1	1	0	0	INIT[12]
1	1	0	1	INIT[13]

Inputs				Outputs
I3	I2	I1	I0	LO
1	1	1	0	INIT[14]
1	1	1	1	INIT[15]

INIT = Binary equivalent of the hexadecimal number assigned to the INIT attribute

Design Entry Method

This design element can be used in schematics.

Available Attributes

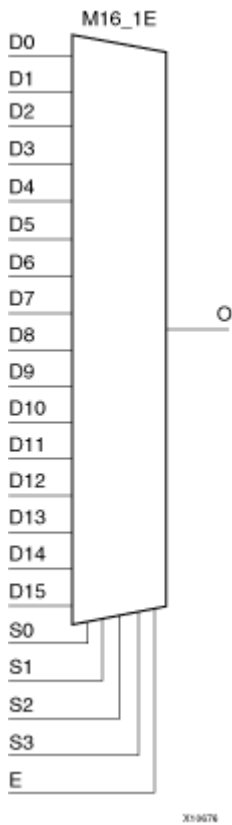
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Initializes look-up tables.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

M16_1E

Macro: 16-to-1 Multiplexer with Enable



Introduction

This design element is a 16-to-1 multiplexer with enable. When the enable input (E) is High, the M16_1E multiplexer chooses one data bit from 16 sources (D15 – D0) under the control of the select inputs (S3 – S0). The output (O) reflects the state of the selected input as shown in the logic table. When (E) is Low, the output is Low.

Logic Table

Inputs						Outputs
E	S3	S2	S1	S0	D15-D0	O
0	X	X	X	X	X	0
1	0	0	0	0	D0	D0
1	0	0	0	1	D1	D1
1	0	0	1	0	D2	D2
1	0	0	1	1	D3	D3
.
.
.
1	1	1	0	0	D12	D12
1	1	1	0	1	D13	D13

Inputs						Outputs
E	S3	S2	S1	S0	D15-D0	O
1	1	1	1	0	D14	D14
1	1	1	1	1	D15	D15

Design Entry Method

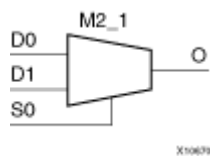
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

M2_1

Macro: 2-to-1 Multiplexer



Introduction

This design element chooses one data bit from two sources (D1 or D0) under the control of the select input (S0). The output (O) reflects the state of the selected data input. When Low, S0 selects D0 and when High, S0 selects D1.

Logic Table

Inputs			Outputs
S0	D1	D0	O
1	D1	X	D1
0	X	D0	D0

Design Entry Method

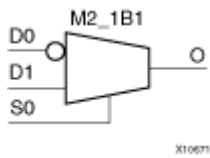
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

M2_1B1

Macro: 2-to-1 Multiplexer with D0 Inverted



Introduction

This design element chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When S0 is Low, the output (O) reflects the inverted value of (D0). When S0 is High, (O) reflects the state of D1.

Logic Table

Inputs			Outputs
S0	D1	D0	O
1	1	X	1
1	0	X	0
0	X	1	0
0	X	0	1

Design Entry Method

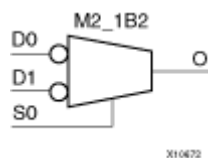
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

M2_1B2

Macro: 2-to-1 Multiplexer with D0 and D1 Inverted



Introduction

This design element chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When S0 is Low, the output (O) reflects the inverted value of D0. When S0 is High, O reflects the inverted value of D1.

Logic Table

Inputs			Outputs
S0	D1	D0	O
1	1	X	0
1	0	X	1
0	X	1	0
0	X	0	1

Design Entry Method

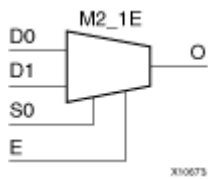
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

M2_1E

Macro: 2-to-1 Multiplexer with Enable



Introduction

This design element is a 2-to-1 multiplexer with enable. When the enable input (E) is High, the M2_1E chooses one data bit from two sources (D1 or D0) under the control of select input (S0). When Low, S0 selects D0 and when High, S0 selects D1. When (E) is Low, the output is Low.

Logic Table

Inputs				Outputs
E	S0	D1	D0	O
0	X	X	X	0
1	0	X	1	1
1	0	X	0	0
1	1	1	X	1
1	1	0	X	0

Design Entry Method

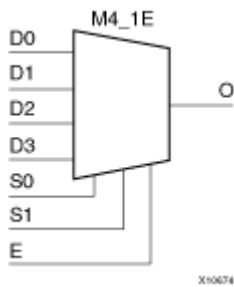
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

M4_1E

Macro: 4-to-1 Multiplexer with Enable



Introduction

This design element is a 4-to-1 multiplexer with enable. When the enable input (E) is High, the M4_1E multiplexer chooses one data bit from four sources (D3, D2, D1, or D0) under the control of the select inputs (S1 – S0). The output (O) reflects the state of the selected input as shown in the logic table. When (E) is Low, the output is Low.

Logic Table

Inputs							Outputs
E	S1	S0	D0	D1	D2	D3	O
0	X	X	X	X	X	X	0
1	0	0	D0	X	X	X	D0
1	0	1	X	D1	X	X	D1
1	1	0	X	X	D2	X	D2
1	1	1	X	X	X	D3	D3

Design Entry Method

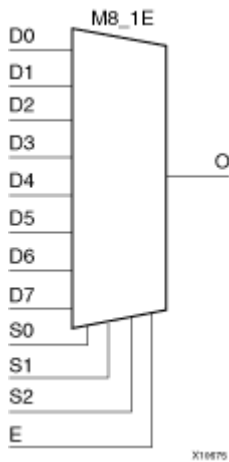
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

M8_1E

Macro: 8-to-1 Multiplexer with Enable



Introduction

This design element is an 8-to-1 multiplexer with enable. When the enable input (E) is High, the M8_1E multiplexer chooses one data bit from eight sources (D7 – D0) under the control of the select inputs (S2 – S0). The output (O) reflects the state of the selected input as shown in the logic table. When (E) is Low, the output is Low.

Logic Table

Inputs				Outputs	
E	S2	S1	S0	D7-D0	O
0	X	X	X	X	0
1	0	0	0	D0	D0
1	0	0	1	D1	D1
1	0	1	0	D2	D2
1	0	1	1	D3	D3
1	1	0	0	D4	D4
1	1	0	1	D5	D5
1	1	1	0	D6	D6
1	1	1	1	D7	D7

Design Entry Method

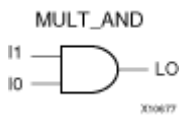
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

MULT_AND

Primitive: Fast Multiplier AND



Introduction

The design element is an AND component located within the slice where the two inputs are shared with the 4-input LUT and the output drives into the carry logic. This added logic is especially useful for building fast and smaller multipliers however be used for other purposes as well. The I1 and I0 inputs must be connected to the I1 and I0 inputs of the associated LUT. The LO output must be connected to the DI input of the associated MUXCY, MUXCY_D, or MUXCY_L.

Logic Table

Inputs		Outputs
I1	I0	LO
0	0	0
0	1	0
1	0	0
1	1	1

Design Entry Method

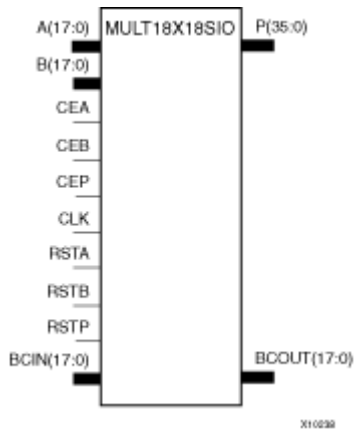
This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

MULT18X18SIO

Primitive: 18 x 18 Cascadable Signed Multiplier with Optional Input and Output Registers, Clock Enable, and Synchronous Reset



Introduction

This design element is a 36-bit output, 18x18-bit input dedicated signed multiplier. This component can perform asynchronous multiplication operations when the attributes AREG, BREG and PREG are all set to 0. Alternatively, synchronous multiplication operations of different latency and performance characteristics can be performed when any combination of those attributes is set to 1. When using the multiplier in synchronous operation, the MULT18X18SIO features active high clock enables for each set of register banks in the multiplier, CEA, CEB and CEP, as well as synchronous resets, RSTA, RSTB, and RSTP. Multiple MULT18X18SIOs can be cascaded to create larger multiplication functions using the BCIN and BCOUT ports in combination with the B_INPUT attribute.

Design Entry Method

This design element can be used in schematics.

Available Attributes

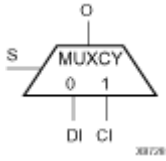
Attribute	Type	Allowed Values	Default	Descriptions
AREG	Integer	0 or 1	1	Specifies the use of the input registers on the A port. A zero disables the use of the register; a one enables the register.
BREG	Integer	0 or 1	1	Specifies the use of the input registers on the B port. A zero disables the use of the register; a one enables the register.
B_INPUT	String	"DIRECT" or "CASCADE"	"DIRECT"	Specifies whether the B port is connected to the general FPGA fabric, "DIRECT" or is connected to the BCOUT port of another MULT18X18SIO.
PREG	Integer	0 or 1	1	Specifies the use of the output registers of the multiplier. A zero disables the use of the register; a one enables the register.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

MUXCY

Primitive: 2-to-1 Multiplexer for Carry Logic with General Output



Introduction

This design element is used to implement a 4-bit high-speed carry propagate function. One such function can be implemented per slice, for a total of 4 bits per configurable logic block (CLB) for Spartan-3A.

The direct input (DI) of a slice is connected to the (DI) input of the MUXCY. The carry in (CI) input of an LC is connected to the CI input of the MUXCY. The select input (S) of the MUXCY is driven by the output of the Look-Up Table (LUT) and configured as a MUX function. The carry out (O) of the MUXCY reflects the state of the selected input and implements the carry out function of each LC. When Low, S selects DI; when High, S selects CI.

The variants “MUXCY_D” and “MUXCY_L” provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

Logic Table

Inputs			Outputs
S	DI	CI	O
0	1	X	1
0	0	X	0
1	X	1	1
1	X	0	0

Design Entry Method

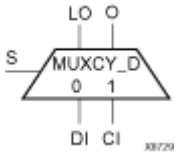
This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

MUXCY_D

Primitive: 2-to-1 Multiplexer for Carry Logic with Dual Output



Introduction

This design element implements a 1-bit, high-speed carry propagate function. One such function can be implemented per logic cell (LC), for a total of 4-bits per configurable logic block (CLB). The direct input (DI) of an LC is connected to the DI input of the MUXCY_D. The carry in (CI) input of an LC is connected to the CI input of the MUXCY_D. The select input (S) of the MUX is driven by the output of the Look-Up Table (LUT) and configured as an XOR function. The carry out (O and LO) of the MUXCY_D reflects the state of the selected input and implements the carry out function of each LC. When Low, S selects \overline{DI} ; when High, S selects CI.

Outputs O and LO are functionally identical. The O output is a general interconnect. See also “MUXCY” and “MUXCY_L”.

Logic Table

Inputs			Outputs	
S	DI	CI	O	LO
0	1	X	1	1
0	0	X	0	0
1	X	1	1	1
1	X	0	0	0

Design Entry Method

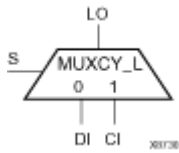
This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

MUXCY_L

Primitive: 2-to-1 Multiplexer for Carry Logic with Local Output



Introduction

This design element implements a 1-bit high-speed carry propagate function. One such function is implemented per logic cell (LC), for a total of 4-bits per configurable logic block (CLB). The direct input (DI) of an LC is connected to the DI input of the MUXCY_L. The carry in (CI) input of an LC is connected to the CI input of the MUXCY_L. The select input (S) of the MUXCY_L is driven by the output of the Look-Up Table (LUT) and configured as an XOR function. The carry out (LO) of the MUXCY_L reflects the state of the selected input and implements the carry out function of each (LC). When Low, (S) selects DI; when High, (S) selects (CI).

See also “MUXCY” and “MUXCY_D.”

Logic Table

Inputs			Outputs
S	DI	CI	LO
0	1	X	1
0	0	X	0
1	X	1	1
1	X	0	0

Design Entry Method

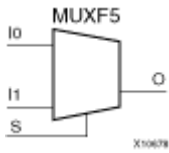
This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

MUXF5

Primitive: 2-to-1 Look-Up Table Multiplexer with General Output



Introduction

This design element provides a multiplexer function in a CLB slice for creating a function-of-5 lookup table or a 4-to-1 multiplexer in combination with the associated lookup tables. The local outputs (LO) from the two lookup tables are connected to the I0 and I1 inputs of the MUXF5. The (S) input is driven from any internal net. When Low, (S) selects I0. When High, (S) selects I1.

The variants, "MUXF5_D" and "MUXF5_L", provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

Logic Table

Inputs			Outputs
S	I0	I1	O
0	1	X	1
0	0	X	0
1	X	1	1
1	X	0	0

Design Entry Method

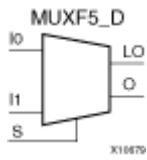
This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

MUXF5_D

Primitive: 2-to-1 Look-Up Table Multiplexer with Dual Output



Introduction

This design element provides a multiplexer function in a CLB slice for creating a function-of-5 lookup table or a 4-to-1 multiplexer in combination with the associated lookup tables. The local outputs (LO) from the two lookup tables are connected to the I0 and I1 inputs of the MUXF5. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

Outputs O and LO are functionally identical. The O output is a general interconnect. The LO output connects to other inputs in the same CLB slice. See also “MUXF5” and “MUXF5_L”

Logic Table

Inputs			Outputs	
S	I0	I1	O	LO
0	1	X	1	1
0	0	X	0	0
1	X	1	1	1
1	X	0	0	0

Design Entry Method

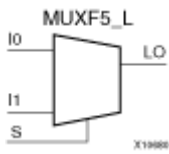
This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

MUXF5_L

Primitive: 2-to-1 Look-Up Table Multiplexer with Local Output



Introduction

This design element provides a multiplexer function in a CLB slice for creating a function-of-5 lookup table or a 4-to-1 multiplexer in combination with the associated lookup tables. The local outputs (LO) from the two lookup tables are connected to the I0 and I1 inputs of the MUXF5. The S input is driven from any internal net. When Low, S selects I0. When High, S selects I1.

The LO output connects to other inputs in the same CLB slice.

See also “MUXF5” and “MUXF5_D”

Logic Table

Inputs			Output
S	I0	I1	LO
0	1	X	1
0	0	X	0
1	X	1	1
1	X	0	0

Design Entry Method

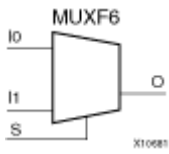
This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

MUXF6

Primitive: 2-to-1 Look-Up Table Multiplexer with General Output



Introduction

This design element provides a multiplexer function in two slices for creating a function-of-6 lookup table or an 8-to-1 multiplexer in combination with the associated four lookup tables and two MUXF5s. The local outputs (LO) from the two MUXF5s in the CLB are connected to the I0 and I1 inputs of the MUXF6. The S input is driven from any internal net. When Low, (S) selects I0. When High, (S) selects I1.

The variants, "MUXF6_D" and "MUXF6_L", provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

Logic Table

Inputs			Outputs
S	I0	I1	O
0	1	X	1
0	0	X	0
1	X	1	1
1	X	0	0

Design Entry Method

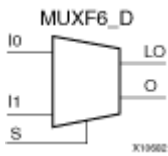
This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

MUXF6_D

Primitive: 2-to-1 Look-Up Table Multiplexer with Dual Output



Introduction

This design element provides a multiplexer function in a two slices for creating a function-of-6 lookup table or an 8-to-1 multiplexer in combination with the associated four lookup tables and two MUXF5s. The local outputs (LO) from the two MUXF5s in the CLB are connected to the I0 and I1 inputs of the MUXF6. The (S) input is driven from any internal net. When Low, (S) selects I0. When High, (S) selects I1.

Outputs (O) and (LO) are functionally identical. The (O) output is a general interconnect. The (LO) output connects to other inputs in the same CLB slice.

Logic Table

Inputs			Outputs	
S	I0	I1	O	LO
0	1	X	1	1
0	0	X	0	0
1	X	1	1	1
1	X	0	0	0

Design Entry Method

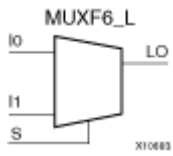
This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

MUXF6_L

Primitive: 2-to-1 Look-Up Table Multiplexer with Local Output



Introduction

This design element provides a multiplexer function for use in creating a function-of-6 lookup table or an 8-to-1 multiplexer in combination with the associated four lookup tables and two MUXF5s. The local outputs (LO) from the two MUXF5s in the (CLB) are connected to the I0 and I1 inputs of the MUXF6. The (S) input is driven from any internal net. When Low, (S) selects I0. When High, (S) selects I1.

The LO output connects to other inputs in the same CLB slice.

Logic Table

Inputs			Output
S	I0	I1	LO
0	1	X	1
0	0	X	0
1	X	1	1
1	X	0	0

Design Entry Method

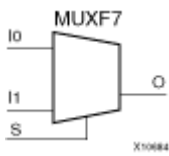
This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

MUXF7

Primitive: 2-to-1 Look-Up Table Multiplexer with General Output



Introduction

This design element provides a multiplexer function for use in creating a function-of-7 Look-Up Table or a 16-to-1 multiplexer in combination with the associated Look-Up Tables. Local outputs (LO) of MUXF6 are connected to the I0 and I1 inputs of the MUXF7. The (S) input is driven from any internal net. When Low, (S) selects I0. When High, (S) selects I1.

The variants, "MUXF7_D" and "MUXF7_L", provide additional types of outputs that can be used by different timing models for more accurate pre-layout timing estimation.

Logic Table

Inputs			Outputs
S	I0	I1	O
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

Port Descriptions

Name	Direction	Width	Function
O	Output	1-Bit	Output of MUX to general routing
I0	Input	1-Bit	Input (tie to MUXF6 LO out)
I1	Input	1-Bit	Input (tie to MUXF6 LO out)
S	Input	1-Bit	Input select to MUX

Design Entry Method

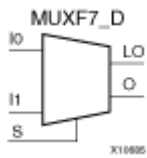
This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

MUXF7_D

Primitive: 2-to-1 Look-Up Table Multiplexer with Dual Output



Introduction

This design element provides a multiplexer function for use in creating a function-of-7 Look-Up Table or a 16-to-1 multiplexer in combination with the associated Look-Up Tables. Local outputs (LO) of MUXF6 are connected to the I0 and I1 inputs of the MUXF7. The S input is driven from any internal net. When Low, (S) selects I0. When High, (S) selects I1.

Outputs O and LO are functionally identical. The O output is a general interconnect. The LO output connects to other inputs in the same CLB slice.

Logic Table

Inputs			Outputs	
S	I0	I1	O	LO
0	I0	X	I0	I0
1	X	I1	I1	I1
X	0	0	0	0
X	1	1	1	1

Port Descriptions

Name	Direction	Width	Function
O	Output	1-Bit	Output of MUX to general routing
LO	Output	1-Bit	Output of MUX to local routing
I0	Input	1-Bit	Input (tie to MUXF6 LO out)
I1	Input	1-Bit	Input (tie to MUXF6 LO out)
S	Input	1-Bit	Input select to MUX

Design Entry Method

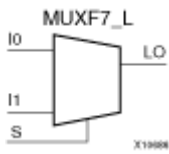
This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

MUXF7_L

Primitive: 2-to-1 Look-Up Table Multiplexer with Local Output



Introduction

This design element provides a multiplexer function for use in creating a function-of-7 Look-Up Table or a 16-to-1 multiplexer in combination with the associated Look-Up Tables. Local outputs (LO) of MUXF6 are connected to the I0 and I1 inputs of the MUXF7. The S input is driven from any internal net. When Low, (S) selects I0. When High, (S) selects I1.

The LO output connects to other inputs in the same CLB slice.

Logic Table

Inputs			Output
S	I0	I1	LO
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

Port Descriptions

Name	Direction	Width	Function
LO	Output	1-Bit	Output of MUX to local routing
I0	Input	1-Bit	Input (tie to MUXF6 LO out)
I1	Input	1-Bit	Input (tie to MUXF6 LO out)
S	Input	1-Bit	Input select to MUX

Design Entry Method

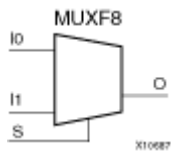
This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

MUXF8

Primitive: 2-to-1 Look-Up Table Multiplexer with General Output



Introduction

This design element provides a multiplexer function in eight slices for creating a function-of-8 Look-Up Table or a 32-to-1 multiplexer in combination with the associated Look-Up Tables, MUXF5s, MUXF6s, and MUXF7s. Local outputs (LO) of MUXF7 are connected to the I0 and I1 inputs of the MUXF8. The S input is driven from any internal net. When Low, (S) selects I0. When High, (S) selects I1.

Logic Table

Inputs			Outputs
S	I0	I1	O
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

Port Descriptions

Name	Direction	Width	Function
O	Output	1-Bit	Output of MUX to general routing
I0	Input	1-Bit	Input (tie to MUXF7 LO out)
I1	Input	1-Bit	Input (tie to MUXF7 LO out)
S	Input	1-Bit	Input select to MUX

Design Entry Method

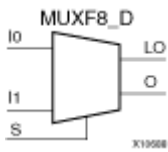
This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

MUXF8_D

Primitive: 2-to-1 Look-Up Table Multiplexer with Dual Output



Introduction

This design element provides a multiplexer function in eight slices for creating a function-of-8 Look-Up Table or a 32-to-1 multiplexer in combination with the associated four Look-Up Tables and two MUXF8s. Local outputs (LO) of MUXF7 are connected to the I0 and I1 inputs of the MUXF8. The S input is driven from any internal net. When Low, (S) selects I0. When High, (S) selects I1.

Outputs O and LO are functionally identical. The O output is a general interconnect. The LO output connects to other inputs in the same CLB slice.

Logic Table

Inputs			Outputs	
S	I0	I1	O	LO
0	I0	X	I0	I0
1	X	I1	I1	I1
X	0	0	0	0
X	1	1	1	1

Port Descriptions

Name	Direction	Width	Function
O	Output	1-Bit	Output of MUX to general routing
LO	Output	1-Bit	Output of MUX to local routing
I0	Input	1-Bit	Input (tie to MUXF7 LO out)
I1	Input	1-Bit	Input (tie to MUXF7 LO out)
S	Input	1-Bit	Input select to MUX

Design Entry Method

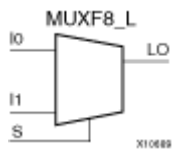
This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

MUXF8_L

Primitive: 2-to-1 Look-Up Table Multiplexer with Local Output



Introduction

This design element provides a multiplexer function in eight slices for creating a function-of-8 Look-Up Table or a 32-to-1 multiplexer in combination with the associated four Look-Up Tables and two MUXF8s. Local outputs (LO) of MUXF7 are connected to the I0 and I1 inputs of the MUXF8. The S input is driven from any internal net. When Low, (S) selects I0. When High, (S) selects I1.

The LO output connects to other inputs in the same CLB slice.

Logic Table

Inputs			Output
S	I0	I1	LO
0	I0	X	I0
1	X	I1	I1
X	0	0	0
X	1	1	1

Port Descriptions

Name	Direction	Width	Function
LO	Output	1-Bit	Output of MUX to local routing
I0	Input	1-Bit	Input (tie to MUXF7 LO out)
I1	Input	1-Bit	Input (tie to MUXF7 LO out)
S	Input	1-Bit	Input select to MUX

Design Entry Method

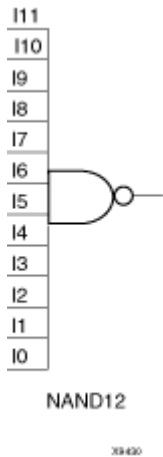
This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND12

Macro: 12- Input NAND Gate with Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

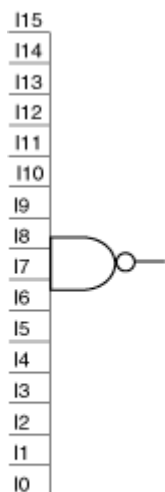
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND16

Macro: 16- Input NAND Gate with Non-Inverted Inputs



NAND16

38421

Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

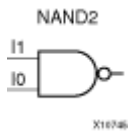
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND2

Primitive: 2-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

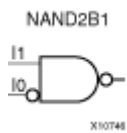
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND2B1

Primitive: 2-Input NAND Gate with 1 Inverted and 1 Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

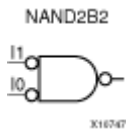
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND2B2

Primitive: 2-Input NAND Gate with Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

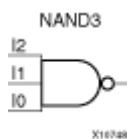
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND3

Primitive: 3-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

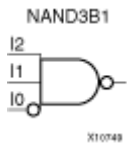
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND3B1

Primitive: 3-Input NAND Gate with 1 Inverted and 2 Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

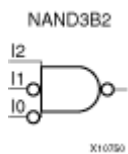
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND3B2

Primitive: 3-Input NAND Gate with 2 Inverted and 1 Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

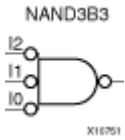
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND3B3

Primitive: 3-Input NAND Gate with Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

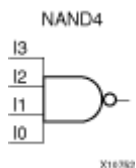
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND4

Primitive: 4-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

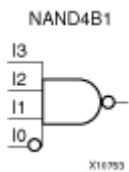
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND4B1

Primitive: 4-Input NAND Gate with 1 Inverted and 3 Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

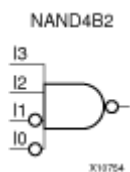
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND4B2

Primitive: 4-Input NAND Gate with 2 Inverted and 2 Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

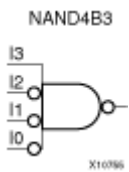
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND4B3

Primitive: 4-Input NAND Gate with 3 Inverted and 1 Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

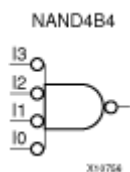
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND4B4

Primitive: 4-Input NAND Gate with Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

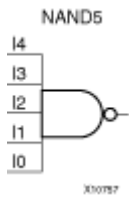
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND5

Primitive: 5-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

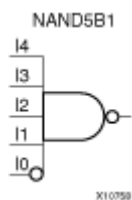
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND5B1

Primitive: 5-Input NAND Gate with 1 Inverted and 4 Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

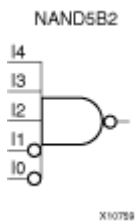
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND5B2

Primitive: 5-Input NAND Gate with 2 Inverted and 3 Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

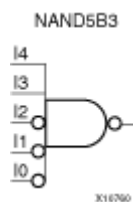
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND5B3

Primitive: 5-Input NAND Gate with 3 Inverted and 2 Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

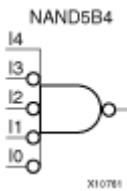
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND5B4

Primitive: 5-Input NAND Gate with 4 Inverted and 1 Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

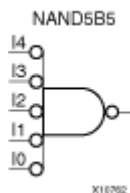
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND5B5

Primitive: 5-Input NAND Gate with Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

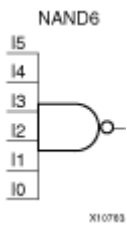
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND6

Macro: 6-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

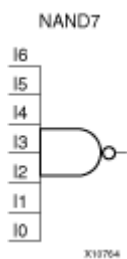
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND7

Macro: 7-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

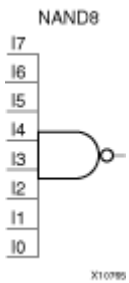
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND8

Macro: 8-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

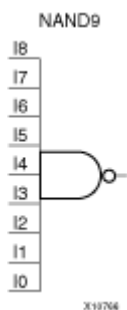
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NAND9

Macro: 9-Input NAND Gate with Non-Inverted Inputs



Introduction

NAND gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NAND gates of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

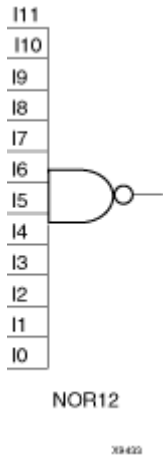
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR12

Macro: 12-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

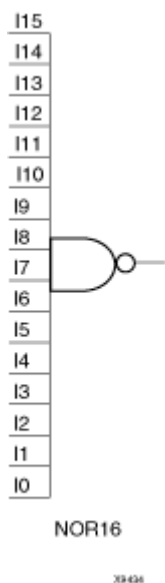
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR16

Macro: 16-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

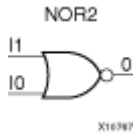
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR2

Primitive: 2-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

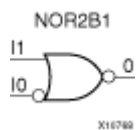
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR2B1

Primitive: 2-Input NOR Gate with 1 Inverted and 1 Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR2B2

Primitive: 2-Input NOR Gate with Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

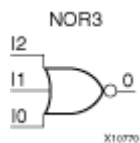
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR3

Primitive: 3-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

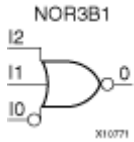
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR3B1

Primitive: 3-Input NOR Gate with 1 Inverted and 2 Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

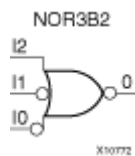
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR3B2

Primitive: 3-Input NOR Gate with 2 Inverted and 1 Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

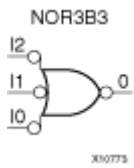
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR3B3

Primitive: 3-Input NOR Gate with Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

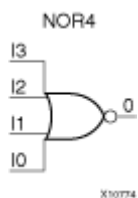
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR4

Primitive: 4-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

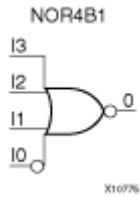
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR4B1

Primitive: 4-Input NOR Gate with 1 Inverted and 3 Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

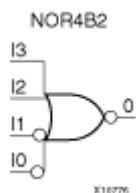
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR4B2

Primitive: 4-Input NOR Gate with 2 Inverted and 2 Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

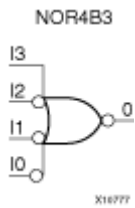
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR4B3

Primitive: 4-Input NOR Gate with 3 Inverted and 1 Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

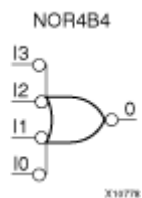
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR4B4

Primitive: 4-Input NOR Gate with Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

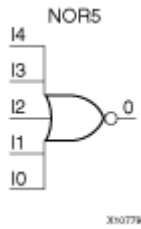
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR5

Primitive: 5-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

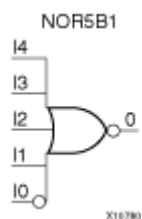
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR5B1

Primitive: 5-Input NOR Gate with 1 Inverted and 4 Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

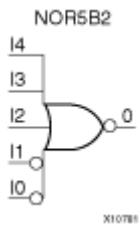
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR5B2

Primitive: 5-Input NOR Gate with 2 Inverted and 3 Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

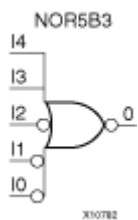
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR5B3

Primitive: 5-Input NOR Gate with 3 Inverted and 2 Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

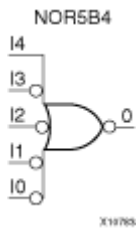
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR5B4

Primitive: 5-Input NOR Gate with 4 Inverted and 1 Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

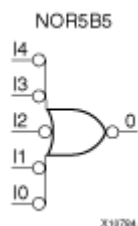
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR5B5

Primitive: 5-Input NOR Gate with Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

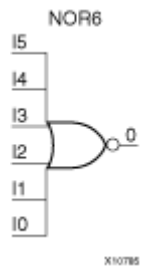
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR6

Macro: 6-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

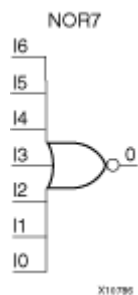
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR7

Macro: 7-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

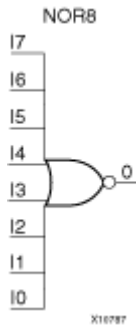
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR8

Macro: 8-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

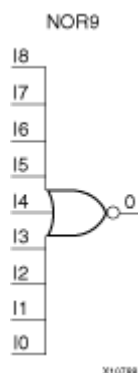
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

NOR9

Macro: 9-Input NOR Gate with Non-Inverted Inputs



Introduction

NOR gates of up to five inputs are available in any combination of inverting and non-inverting inputs. NOR gates of six to nine inputs, 12 inputs, and 16 inputs are available only with non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace gates with unused inputs with gates having the necessary number of inputs.

Design Entry Method

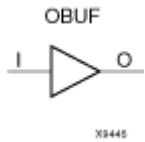
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OBUF

Primitive: Output Buffer



Introduction

This design element is a simple output buffer used to drive output signals to the FPGA device pins that do not need to be 3-stated (constantly driven). Either an OBUF, OBUFT, OBUFDS, or OBUFTDS must be connected to every output port in the design.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVTTTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

Port Descriptions

Name	Direction	Width	Function
O	Output	1-bit	Output of OBUF to be connected directly to top-level output port.
I	Input	1-bit	Input of OBUF. Connect to the logic driving the output port.

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	Consult the product Data Sheet.	"DEFAULT"	Specifies the I/O standard to be used for this output.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OBUF16

Macro: 16-Bit Output Buffer



Introduction

This design element is a multiple output buffer.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVTTTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

This design element can be used in schematics.

Available Attributes

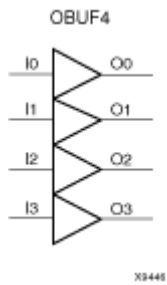
Attribute	Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	Consult the product Data Sheet.	"DEFAULT"	Specifies the I/O standard to be used for this output.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OBUF4

Macro: 4-Bit Output Buffer



Introduction

This design element is a multiple output buffer.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVTTTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	Consult the product Data Sheet.	"DEFAULT"	Specifies the I/O standard to be used for this output.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OBUF8

Macro: 8-Bit Output Buffer



Introduction

This design element is a multiple output buffer.

This element isolates the internal circuit and provides drive current for signals leaving a chip. It exists in input/output blocks (IOB). Its output (O) is connected to an OPAD or an IOPAD. The interface standard used by this element is LVTTTL. Also, this element has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

This design element can be used in schematics.

Available Attributes

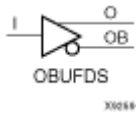
Attribute	Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	Consult the product Data Sheet.	"DEFAULT"	Specifies the I/O standard to be used for this output.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OBUFDS

Primitive: Differential Signaling Output Buffer



Introduction

This design element is a single output buffer that supports low-voltage, differential signaling (1.8 v CMOS). OBUFDS isolates the internal circuit and provides drive current for signals leaving the chip. Its output is represented as two distinct ports (O and OB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET and MYNETB).

Logic Table

Inputs		Outputs
I	O	OB
0	0	1
1	1	0

Port Descriptions

Name	Direction	Width	Function
O	Output	1-Bit	Diff_p output (connect directly to top level port)
OB	Input	1-Bit	Diff_n output (connect directly to top level port)
I	Input	1-Bit	Buffer input

Design Entry Method

This design element can be used in schematics.

Available Attributes

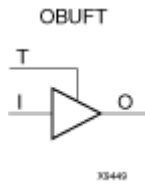
Attribute	Type	Allowed Values	Default	Descriptions
IOSTANDARD	String	"DEFAULT"	"DEFAULT"	Use to assign an I/O standard to an I/O primitive.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OBUFT

Primitive: 3-State Output Buffer with Active Low Output Enable



Introduction

This design element is a single, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTTTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

Inputs		Outputs
T	I	O
1	X	Z
0	I	F

Port Descriptions

Name	Direction	Width	Function
O	Output	1-Bit	Buffer output (connect directly to top-level port)
I	Input	1-Bit	Buffer input
T	Input	1-Bit	3-state enable input

Design Entry Method

This design element can be used in schematics.

Available Attributes

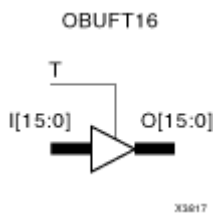
Attribute	Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	Consult the product Data Sheet.	"DEFAULT"	Specifies the I/O standard to be used for this output.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OBUFT16

Macro: 16-Bit 3-State Output Buffer with Active Low Output Enable



Introduction

This design element is a multiple, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTTTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

Inputs		Outputs
T	I	O
1	X	Z
0	I	F

Design Entry Method

This design element is only for use in schematics.

Available Attributes

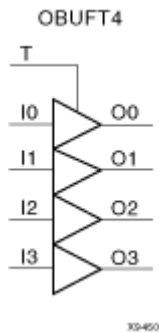
Attribute	Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	Consult the product Data Sheet.	"DEFAULT"	Specifies the I/O standard to be used for this output.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OBUFT4

Macro: 4-Bit 3-State Output Buffers with Active-Low Output Enable



Introduction

This design element is a multiple, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

Inputs		Outputs
T	I	O
1	X	Z
0	I	F

Design Entry Method

This design element is only for use in schematics.

Available Attributes

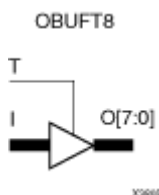
Attribute	Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	Consult the product Data Sheet.	"DEFAULT"	Specifies the I/O standard to be used for this output.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OBUFT8

Macro: 8-Bit 3-State Output Buffers with Active-Low Output Enable



Introduction

This design element is a multiple, 3-state output buffer with input I, output O, and active-Low output enables (T). This element uses the LVTTL standard and has selectable drive and slew rates using the DRIVE and SLOW or FAST constraints. The defaults are DRIVE=12 mA and SLOW slew.

When T is Low, data on the inputs of the buffers is transferred to the corresponding outputs. When T is High, the output is high impedance (off or Z state). OBUFTs are generally used when a single-ended output is needed with a 3-state capability, such as the case when building bidirectional I/O.

Logic Table

Inputs		Outputs
T	I	O
1	X	Z
0	I	F

Design Entry Method

This design element is only for use in schematics.

Available Attributes

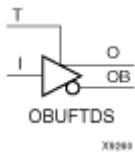
Attribute	Type	Allowed Values	Default	Description
DRIVE	Integer	2, 4, 6, 8, 12, 16, 24	12	Specifies the output current drive strength of the I/O. It is suggested that you set this to the lowest setting tolerable for the design drive and timing requirements.
IOSTANDARD	String	Consult the product Data Sheet.	"DEFAULT"	Specifies the I/O standard to be used for this output.
SLEW	String	"SLOW" or "FAST"	"SLOW"	Specifies the slew rate of the output driver. Consult the product Data Sheet for recommendations of the best setting for this attribute.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OBUFTDS

Primitive: 3-State Output Buffer with Differential Signaling, Active-Low Output Enable



Introduction

This design element is an output buffer that supports low-voltage, differential signaling. For the OBUFTDS, a design level interface signal is represented as two distinct ports (O and OB), one deemed the "master" and the other the "slave." The master and the slave are opposite phases of the same logical signal (for example, MYNET_P and MYNET_N).

Logic Table

Inputs		Outputs	
I	T	O	OB
X	1	Z	Z
0	0	0	1
1	0	1	0

Port Descriptions

Name	Direction	Width	Function
O	Output	1-Bit	Diff_p output (connect directly to top level port)
OB	Output	1-Bit	Diff_n output (connect directly to top level port)
I	Input	1-Bit	Buffer input
T	Input	1-Bit	3-state enable input

Design Entry Method

This design element can be used in schematics.

Available Attributes

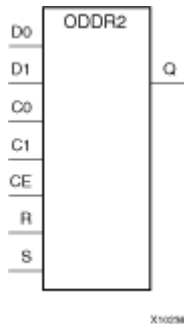
Attribute	Type	Allowed Values	Default	Descriptions
IOSTANDARD	String	"DEFAULT"	"DEFAULT"	Use to assign an I/O standard to an I/O primitive.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ODDR2

Primitive: Dual Data Rate Output D Flip-Flop with Optional Data Alignment, Clock Enable and Programmable Synchronous or Asynchronous Set/Reset



Introduction

The design element is an output double data rate (DDR) register useful in producing double data rate signals exiting the FPGA. The ODDR2 requires two clocks (C0 and C1) to be connected to the component so that data is provided at the positive edge of both clocks. The ODDR2 features an active high clock enable port, CE, which can be used to suspend the operation of the registers and both set and reset ports that can be configured to be synchronous or asynchronous to the respective clocks. The ODDR2 has an optional alignment feature, which allows data to be captured by a single clock and clocked out by two clocks.

Logic Table

Inputs							Outputs
S	R	CE	D0	D1	C0	C1	O
1	X	X	X	X	X	X	1
0	1	X	X	X	X	X	not INIT
0	0	0	X	X	X	X	No Change
0	0	1	D0	X	Rising	X	D0
0	0	1	X	D1	X	Rising	D1

Set/Reset can be synchronous via SRTYPE value

Design Entry Method

This design element can be used in schematics.

Available Attributes

Attribute	Type	Allowed Values	Default	Descriptions
DDR_ALIGNMENT	String	"NONE", "C0" or "C1"	"NONE"	Sets the input capture behavior for the DDR register. "NONE" clocks in data to the D0 input on the positive transition of the C0 clock and D1 on the positive transition of the C1 clock. "C0" allows the input clocking of both D0 and D1 align to the positive edge of the C0 clock. "C1" allows the input clocking of both D0 and D1 align to the positive edge of the C1 clock.

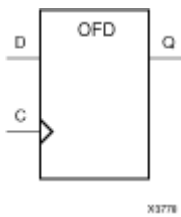
Attribute	Type	Allowed Values	Default	Descriptions
INIT	Integer	0 or 1	0	Sets initial state of the Q0 output to 0 or 1.
SRTYPE	String	"SYNC" or "ASYNC"	"SYNC"	Specifies "SYNC" or "ASYNC" set/reset.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFD

Macro: Output D Flip-Flop



Introduction

This design element is a single output D flip-flop.

The outputs are connected to OPADs or IOPADs. The data on the (D) inputs is loaded into the flip-flops during the Low-to-High clock (C) transition and appears on the (Q) outputs.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
D	C	Q
D	↑	D

Design Entry Method

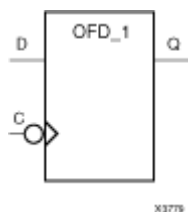
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFD_1

Macro: Output D Flip-Flop with Inverted Clock



Introduction

The design element is located in an input/output block (IOB). The output (Q) of the D flip-flop is connected to an OPAD or an IOPAD. The data on the (D) input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the (Q) output.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
D	C	Q
D	↓	D

Design Entry Method

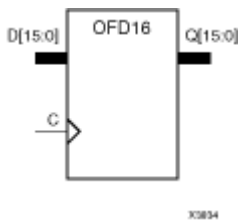
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFD16

Macro: 16-Bit Output D Flip-Flop



Introduction

This design element is a multiple output D flip-flop.

The outputs are connected to OPADs or IOPADs. The data on the (D) inputs is loaded into the flip-flops during the Low-to-High clock (C) transition and appears on the (Q) outputs.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
D	C	Q
D	↑	D

Design Entry Method

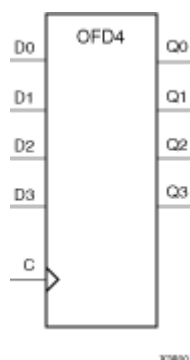
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFD4

Macro: 4-Bit Output D Flip-Flop



Introduction

This design element is a multiple output D flip-flop.

The outputs are connected to OPADs or IOPADs. The data on the (D) inputs is loaded into the flip-flops during the Low-to-High clock (C) transition and appears on the (Q) outputs.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
D	C	Q
D	↑	D

Design Entry Method

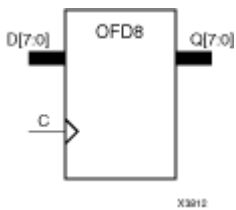
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFD8

Macro: 8-Bit Output D Flip-Flop



Introduction

This design element is a multiple output D flip-flop.

The outputs are connected to OPADs or IOPADs. The data on the (D) inputs is loaded into the flip-flops during the Low-to-High clock (C) transition and appears on the (Q) outputs.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
D	C	Q
D	↑	D

Design Entry Method

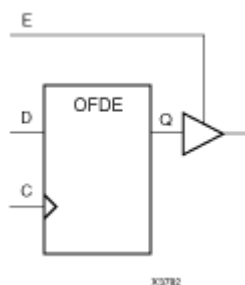
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFDE

Macro: D Flip-Flop with Active-High Enable Output Buffers



Introduction

This is a single D flip-flop whose output is enabled by a 3-state buffer. The flip-flop data output (Q) is connected to the input of output buffer (OBUFE). The OBUFE output (O) is connected to an OPAD or IOPAD. The data on the data input (D) is loaded into the flip-flop during the Low-to-High clock (C) transition. When the active-High enable input (E) is High, the data on the flip-flop output (Q) appears on the OBUFE (O) output. When (E) is Low, the output is high impedance (Z state or Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Output
E	D	C	O
0	X	X	Z
1	Dn	↑	Dn

Design Entry Method

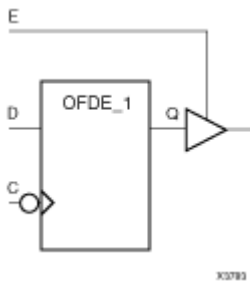
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFDE_1

Macro: D Flip-Flop with Active-High Enable Output Buffer and Inverted Clock



Introduction

This design element and its output buffer are located in an input/output block (IOB). The data output of the flip-flop (Q) is connected to the input of an output buffer or OBUFE. The output of the OBUFE is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-High enable input (E) is High, the data on the flip-flop output (Q) appears on the (O) output. When (E) is Low, the output is high impedance (Z state or Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
E	D	C	O
0	X	X	Z
1	D	↓	D

Design Entry Method

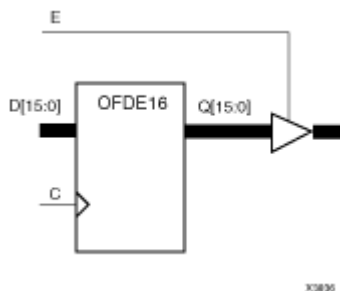
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFDE16

Macro: 16-Bit D Flip-Flop with Active-High Enable Output Buffers



Introduction

This is a multiple D flip-flop whose outputs are enabled by 3-state buffers. The flip-flop data outputs (Q) are connected to the inputs of output buffers (OBUFE). The OBUFE outputs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-High enable inputs (E) are High, the data on the flip-flop outputs (Q) appears on the OBUFE outputs (O). When (E) is Low, outputs are high impedance (Z state or Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
E	D	C	O
0	X	X	Z
1	Dn	↑	Dn

Design Entry Method

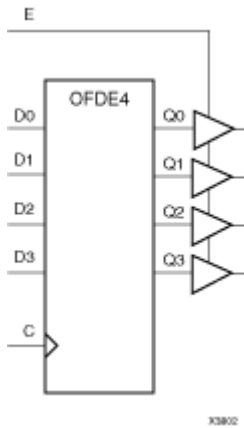
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFDE4

Macro: 4-Bit D Flip-Flop with Active-High Enable Output Buffers



Introduction

This is a multiple D flip-flop whose outputs are enabled by 3-state buffers. The flip-flop data outputs (Q) are connected to the inputs of output buffers (OBUFE). The OBUFE outputs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-High enable inputs (E) are High, the data on the flip-flop outputs (Q) appears on the OBUFE outputs (O). When (E) is Low, outputs are high impedance (Z state or Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
E	D	C	O
0	X	X	Z
1	D _n	↑	D _n

Design Entry Method

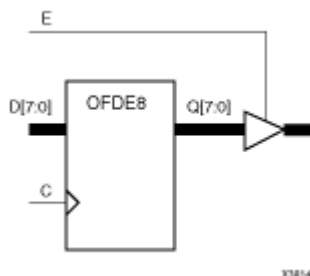
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFDE8

Macro: 8-Bit D Flip-Flop with Active-High Enable Output Buffers



Introduction

This is a multiple D flip-flop whose outputs are enabled by 3-state buffers. The flip-flop data outputs (Q) are connected to the inputs of output buffers (OBUFE). The OBUFE outputs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-High enable inputs (E) are High, the data on the flip-flop outputs (Q) appears on the OBUFE outputs (O). When (E) is Low, outputs are high impedance (Z state or Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
E	D	C	O
0	X	X	Z
1	Dn	↑	Dn

Design Entry Method

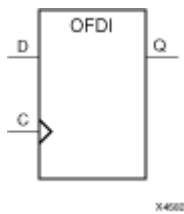
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFDI

Macro: Output D Flip-Flop (Asynchronous Preset)



Introduction

The design element is contained in an input/output block (IOB). The output (Q) of the (D) flip-flop is connected to an OPAD or an IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q).

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs		Outputs
D	C	Q
D	↑	D

Design Entry Method

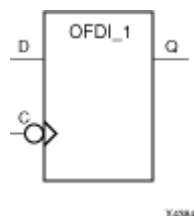
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFDI_1

Macro: Output D Flip-Flop with Inverted Clock (Asynchronous Preset)



Introduction

This design element exists in an input/output block (IOB). The (D) flip-flop output (Q) is connected to an OPAD or an IOPAD. The data on the (D) input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the (Q) output.

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs		Outputs
D	C	Q
D	↓	D

Design Entry Method

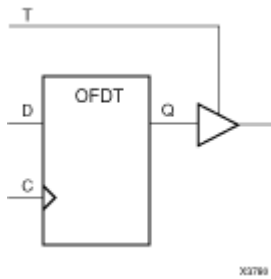
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFTD

Macro: D Flip-Flop with Active-Low 3-State Output Buffer



Introduction

This design element is a single D flip-flops whose output is enabled by a 3-state buffer.

The data outputs (Q) of the flip-flops are connected to the inputs of output buffers (OBUFT). The outputs of the OBUFTs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-Low enable inputs (T) are Low, the data on the flip-flop outputs (Q) appears on the (O) outputs. When (T) is High, outputs are high impedance (Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
T	D	C	O
1	X	X	Z
0	D	↑	D

Design Entry Method

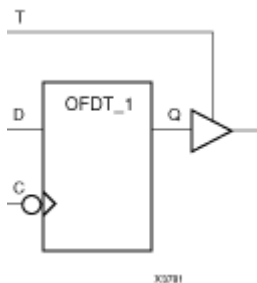
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFDT_1

Macro: D Flip-Flop with Active-Low 3-State Output Buffer and Inverted Clock



Introduction

The design element and its output buffer are located in an input/output block (IOB). The flip-flop data output (Q) is connected to the input of an output buffer (OBUFT). The OBUFT output is connected to an OPAD or an IOPAD. The data on the data input (D) is loaded into the flip-flop on the High-to-Low clock (C) transition. When the active-Low enable input (T) is Low, the data on the flip-flop output (Q) appears on the (O) output. When (T) is High, the output is high impedance (Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
T	D	C	O
1	X	X	Z
0	D	↓	D

Design Entry Method

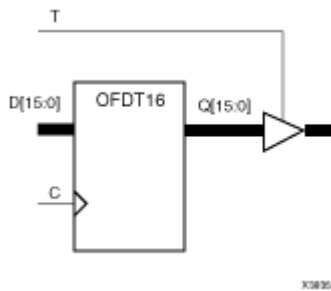
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFDT16

Macro: 16-Bit D Flip-Flop with Active-Low 3-State Output Buffers



Introduction

This design element is a multiple D flip-flop whose output are enabled by 3-state buffers.

The data outputs (Q) of the flip-flops are connected to the inputs of output buffers (OBUFT). The outputs of the OBUFTs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-Low enable inputs (T) are Low, the data on the flip-flop outputs (Q) appears on the (O) outputs. When (T) is High, outputs are high impedance (Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
T	D	C	O
1	X	X	Z
0	D	↑	D

Design Entry Method

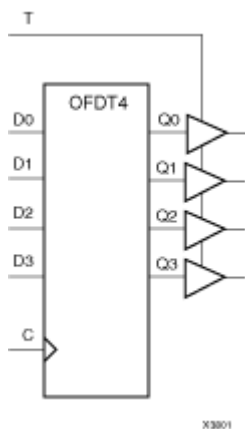
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFDT4

Macro: 4-Bit D Flip-Flop with Active-Low 3-State Output Buffers



Introduction

This design element is a multiple D flip-flop whose output are enabled by 3-state buffers.

The data outputs (Q) of the flip-flops are connected to the inputs of output buffers (OBUFT). The outputs of the OBUFTs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-Low enable inputs (T) are Low, the data on the flip-flop outputs (Q) appears on the (O) outputs. When (T) is High, outputs are high impedance (Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
T	D	C	O
1	X	X	Z
0	D	↑	D

Design Entry Method

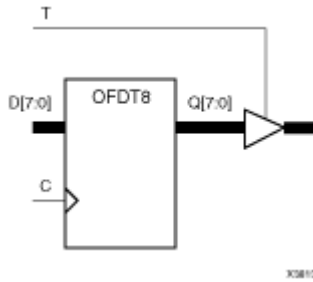
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFDT8

Macro: 8-Bit D Flip-Flop with Active-Low 3-State Output Buffers



Introduction

This design element is a multiple D flip-flop whose output are enabled by 3-state buffers.

The data outputs (Q) of the flip-flops are connected to the inputs of output buffers (OBUFT). The outputs of the OBUFTs (O) are connected to OPADs or IOPADs. The data on the data inputs (D) is loaded into the flip-flops during the Low-to-High clock (C) transition. When the active-Low enable inputs (T) are Low, the data on the flip-flop outputs (Q) appears on the (O) outputs. When (T) is High, outputs are high impedance (Off).

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
T	D	C	O
1	X	X	Z
0	D	↑	D

Design Entry Method

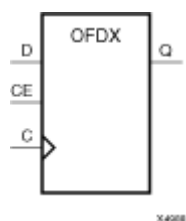
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFDX

Macro: Output D Flip-Flop with Clock Enable



Introduction

This design element is a single output D flip-flop. The (Q) output is connected to OPAD or IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears on the (Q) output. When (CE) is Low, the flip-flop output does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	Dn	↑	Dn
0	X	X	No change

Design Entry Method

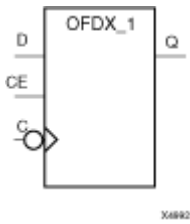
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFDX_1

Macro: Output D Flip-Flop with Inverted Clock and Clock Enable



Introduction

The design element is located in an input/output block (IOB). The output (Q) of the (D) flip-flop is connected to an OPAD or an IOPAD. The data on the (D) input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the (Q) output. When the (CE) pin is Low, the output (Q) does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	D	↓	D
0	X	X	No Change

Design Entry Method

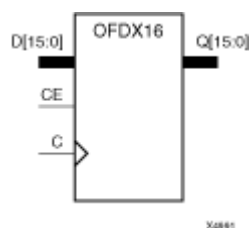
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFDX16

Macro: 16-Bit Output D Flip-Flop with Clock Enable



Introduction

This design element is a multiple output D flip-flop. The (Q) output is connected to OPAD or IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears on the (Q) output. When (CE) is Low, the flip-flop output does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	Dn	↑	Dn
0	X	X	No change

Design Entry Method

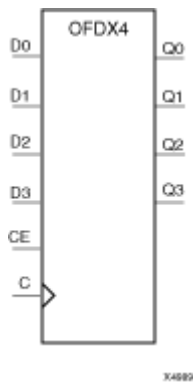
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFDX4

Macro: 4-Bit Output D Flip-Flop with Clock Enable



Introduction

This design element is a multiple output D flip-flop. The (Q) output is connected to OPAD or IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears on the (Q) output. When (CE) is Low, the flip-flop output does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	Dn	↑	Dn
0	X	X	No change

Design Entry Method

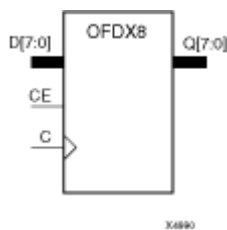
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFDX8

Macro: 8-Bit Output D Flip-Flop with Clock Enable



Introduction

This design element is a multiple output D flip-flop. The (Q) output is connected to OPAD or IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears on the (Q) output. When (CE) is Low, the flip-flop output does not change.

This flip-flop is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	Dn	↑	Dn
0	X	X	No change

Design Entry Method

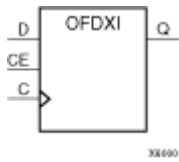
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFDXI

Macro: Output D Flip-Flop with Clock Enable (Asynchronous Preset)



Introduction

The design element is contained in an input/output block (IOB). The output (Q) of the D flip-flop is connected to an OPAD or an IOPAD. The data on the (D) input is loaded into the flip-flop during the Low-to-High clock (C) transition and appears at the output (Q). When (CE) is Low, the output does not change

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	D	↑	D
0	X	X	No Change

Design Entry Method

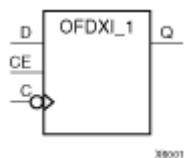
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OFDXI_1

Macro: Output D Flip-Flop with Inverted Clock and Clock Enable (Asynchronous Preset)



Introduction

The design element is located in an input/output block (IOB). The D flip-flop output (Q) is connected to an OPAD or an IOPAD. The data on the D input is loaded into the flip-flop during the High-to-Low clock (C) transition and appears on the Q output. When CE is Low, the output (Q) does not change.

This flip-flop is asynchronously preset, output High, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs			Outputs
CE	D	C	Q
1	D	↓	D
0	X	X	No Change

Design Entry Method

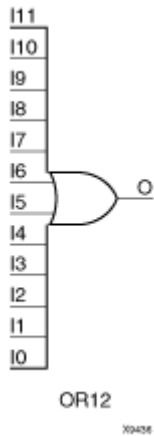
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR12

Macro: 12-Input OR Gate with Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

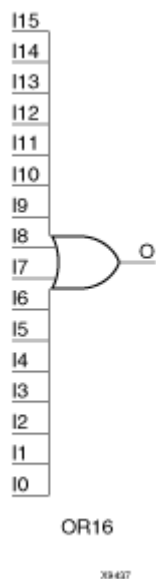
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR16

Macro: 16-Input OR Gate with Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

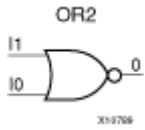
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR2

Primitive: 2-Input OR Gate with Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

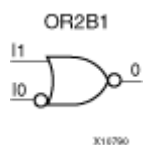
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR2B1

Primitive: 2-Input OR Gate with 1 Inverted and 1 Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

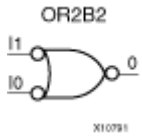
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR2B2

Primitive: 2-Input OR Gate with Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

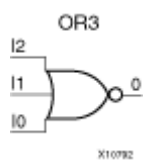
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR3

Primitive: 3-Input OR Gate with Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

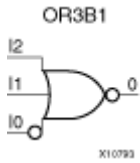
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR3B1

Primitive: 3-Input OR Gate with 1 Inverted and 2 Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

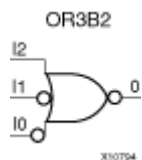
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR3B2

Primitive: 3-Input OR Gate with 2 Inverted and 1 Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

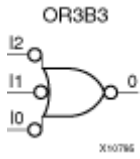
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR3B3

Primitive: 3-Input OR Gate with Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

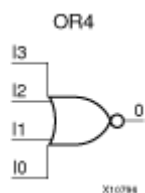
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR4

Primitive: 4-Input OR Gate with Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

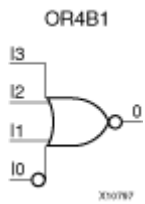
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR4B1

Primitive: 4-Input OR Gate with 1 Inverted and 3 Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

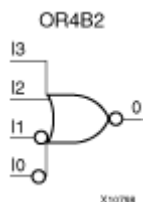
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR4B2

Primitive: 4-Input OR Gate with 2 Inverted and 2 Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

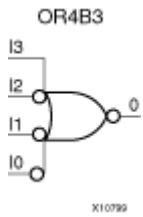
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR4B3

Primitive: 4-Input OR Gate with 3 Inverted and 1 Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

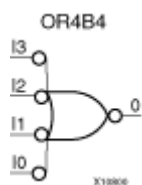
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR4B4

Primitive: 4-Input OR Gate with Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

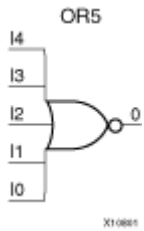
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR5

Primitive: 5-Input OR Gate with Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

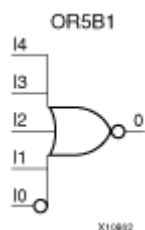
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR5B1

Primitive: 5-Input OR Gate with 1 Inverted and 4 Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

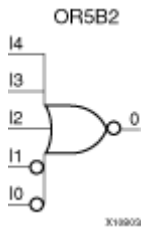
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR5B2

Primitive: 5-Input OR Gate with 2 Inverted and 3 Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

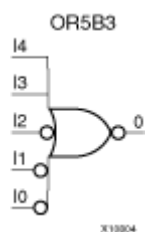
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR5B3

Primitive: 5-Input OR Gate with 3 Inverted and 2 Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

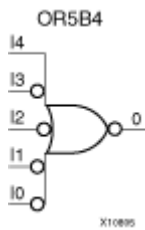
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR5B4

Primitive: 5-Input OR Gate with 4 Inverted and 1 Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

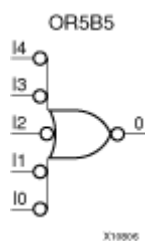
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR5B5

Primitive: 5-Input OR Gate with Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

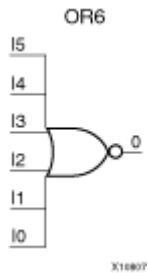
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR6

Macro: 6-Input OR Gate with Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

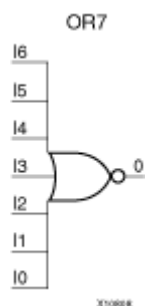
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR7

Macro: 7-Input OR Gate with Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

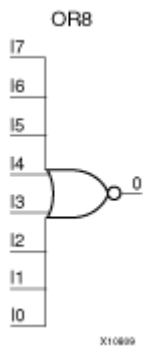
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR8

Macro: 8-Input OR Gate with Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

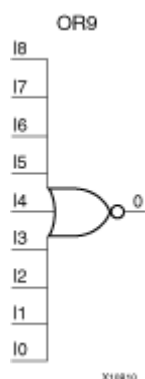
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

OR9

Macro: 9-Input OR Gate with Non-Inverted Inputs



Introduction

OR functions of up to five inputs are available in any combination of inverting and non-inverting inputs. OR functions of six to nine inputs, 12 inputs, and 16 inputs are available with only non-inverting inputs. To invert some or all inputs, use external inverters. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

PULLDOWN

Primitive: Resistor to GND for Input Pads, Open-Drain, and 3-State Outputs

PULLDOWN



Introduction

This resistor element is connected to input, output, or bidirectional pads to guarantee a logic Low level for nodes that might float.

Port Descriptions

Name	Direction	Width	Function
O	Output	1-Bit	Pulldown output (connect directly to top level port)

Design Entry Method

This design element can be used in schematics.

This element can be connected to a net in the following locations on a top-level schematic file:

- A net connected to an input IO Marker
- A net connected to both an output IO Marker and 3-statable IO element, such as an OBUFT.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

PULLUP

Primitive: Resistor to VCC for Input PADS, Open-Drain, and 3-State Outputs



Introduction

This design element allows for an input, 3-state output or bi-directional port to be driven to a weak high value when not being driven by an internal or external source. This element establishes a High logic level for open-drain elements and macros when all the drivers are off.

Port Descriptions

Name	Direction	Width	Function
O	Output	1-Bit	Pullup output (connect directly to top level port)

Design Entry Method

This design element can be used in schematics.

This element can be connected to a net in the following locations on a top-level schematic file:

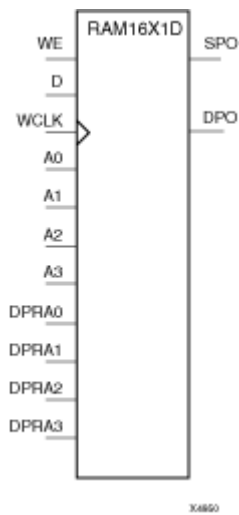
- A net connected to an input IO Marker
- A net connected to both an output IO Marker and 3-statable IO element, such as an OBUFT.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

RAM16X1D

Primitive: 16-Deep by 1-Wide Static Dual Port Synchronous RAM



Introduction

This element is a 16-word by 1-bit static dual port random access memory with synchronous write capability. The device has two address ports: the read address (DPRA3 – DPRA0) and the write address (A3 – A0). These two address ports are asynchronous. The read address controls the location of the data driven out of the output pin (DPO), and the write address controls the destination of a valid write transaction. When the write enable (WE) is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected.

When WE is High, any positive transition on (WCLK) loads the data on the data input (D) into the word selected by the 4-bit write address. For predictable performance, write address and data inputs must be stable before a Low-to-High (WCLK) transition. This RAM block assumes an active-High (WCLK). (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

The SPO output reflects the data in the memory cell addressed by A3 – A0. The DPO output reflects the data in the memory cell addressed by DPRA3 – DPRA0.

Note The write process is not affected by the address on the read address port.

You can use the INIT attribute to directly specify an initial value. The value must be a hexadecimal number, for example, INIT=ABAC. If the INIT attribute is not specified, the RAM is initialized with all zeros.

Logic Table

Mode selection is shown in the following logic table:

Inputs			Outputs	
WE (mode)	WCLK	D	SPO	DPO
0 (read)	X	X	data_a	data_d
1 (read)	0	X	data_a	data_d
1 (read)	1	X	data_a	data_d
1 (write)	↑	D	D	data_d

Inputs			Outputs	
WE (mode)	WCLK	D	SPO	DPO
1 (read)	↓	X	data_a	data_d
data_a = word addressed by bits A3-A0 data_d = word addressed by bits DPRA3-DPRA0				

Design Entry Method

This design element can be used in schematics.

Available Attributes

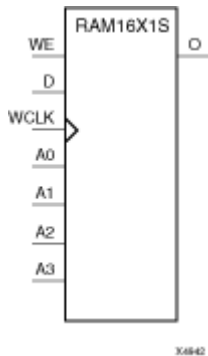
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros.	Initializes RAMs, registers, and look-up tables.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

RAM16X1S

Primitive: 16-Deep by 1-Wide Static Synchronous RAM



Introduction

This element is a 16-word by 1-bit static random access memory with synchronous write capability. When the write enable (WE) is set Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is set High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 4-bit address (A3 – A0). This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins. You can initialize RAM16X1S during configuration using the INIT attribute.

Logic Table

Inputs			Outputs
WE(mode)	WCLK	D	O
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D	D
1 (read)	↓	X	Data

Data = word addressed by bits A3 – A0

Design Entry Method

This design element can be used in schematics.

Available Attributes

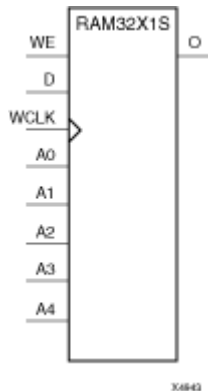
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Specifies initial contents of the RAM.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

RAM32X1S

Primitive: 32-Deep by 1-Wide Static Synchronous RAM



Introduction

The design element is a 32-word by 1-bit static random access memory with synchronous write capability. When the write enable is Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When (WE) is High, any positive transition on (WCLK) loads the data on the data input (D) into the word selected by the 5-bit address (A4 A0). For predictable performance, address and data inputs must be stable before a Low-to-High (WCLK) transition. This RAM block assumes an active-High (WCLK). However, (WCLK) can be active-High or active-Low. Any inverter placed on the (WCLK) input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins. You can initialize RAM32X1S during configuration using the INIT attribute.

Logic Table

Inputs			Outputs
WE (Mode)	WCLK	D	O
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↓	D	D
1 (read)	↑	X	Data

Design Entry Method

This design element can be used in schematics.

Available Attributes

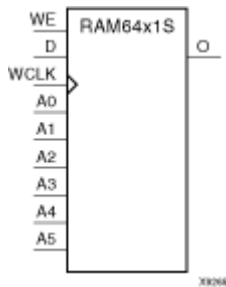
Attribute	Type	Allowed Values	Default	Descriptions
INIT	Hexadecimal	Any 32-Bit Value	All zeros	Specifies initial contents of the RAM.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

RAM64X1S

Primitive: 64-Deep by 1-Wide Static Synchronous RAM



Introduction

This design element is a 64-word by 1-bit static random access memory (RAM) with synchronous write capability. When the write enable is set Low, transitions on the write clock (WCLK) are ignored and data stored in the RAM is not affected. When WE is set High, any positive transition on WCLK loads the data on the data input (D) into the word selected by the 6-bit address (A5 - A0). This RAM block assumes an active-High WCLK. However, WCLK can be active-High or active-Low. Any inverter placed on the WCLK input net is absorbed into the block.

The signal output on the data output pin (O) is the data that is stored in the RAM at the location defined by the values on the address pins.

You can initialize this element during configuration using the INIT attribute.

Logic Table

Mode selection is shown in the following logic table

Inputs			Outputs
WE (mode)	WCLK	D	O
0 (read)	X	X	Data
1 (read)	0	X	Data
1 (read)	1	X	Data
1 (write)	↑	D	D
1 (read)	↓	X	Data

Data = word addressed by bits A5 – A0

Design Entry Method

This design element can be used in schematics.

Available Attributes

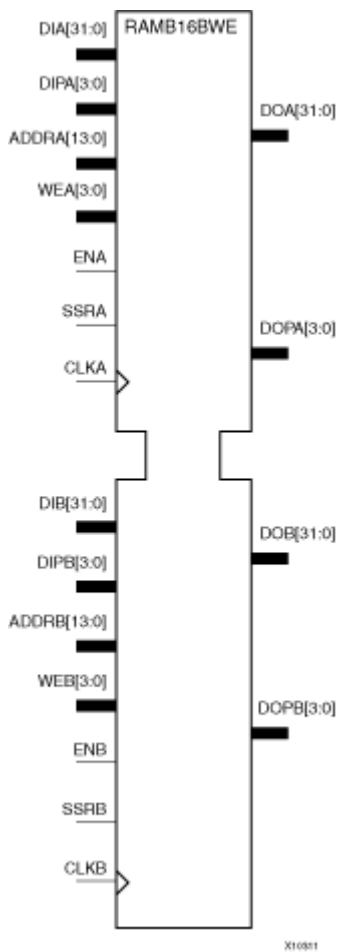
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Initializes ROMs, RAMs, registers, and look-up tables.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

RAMB16BWE

Primitive: 16K-bit Data and 2K-bit Parity Configurable Synchronous Dual Port Block RAM



Introduction

This design element can be configured and used as a 1-bit wide by 16K deep to a 36-bit wide by 512 deep single-port or dual port RAM. Both read and write operations are fully synchronous to the supplied clock(s) to the component however Port A and Port B may operate fully independent and asynchronous to each other accessing the same memory array. When configured in the wider data width modes, byte-enable write operations are possible. This Block RAM memory offers fast and flexible storage of large amounts of on-chip data.

Port Descriptions

Name	Direction	Width (Bits)	Function
DOA, DOB	Output	32-bits	Port A/B data output bus.
DOPA, DOPB	Output	4-bits	Port A/B parity output bus.
DIA, DIB	Input	32-bits	Port A/B data input bus.
DIPA, DIPB	Input	4-bits	Port A/B parity input bus.

Name	Direction	Width (Bits)	Function
ADDRA[13:5], ADDR[13:5]	Input	14-bits	Port A/B address input bus. LSB always exists on ADDRA/B[0] while the MSB is determined by the settings for DATA_WIDTH_A/B.
WEA[0:0], WEB[0:0]	Input	4-bits	Port A/B byte-wide write enable.
ENA, ENB	Input	1-bit	Port A/B enable
SSRA, SSRB	Input	1-bit	Port A/B output registers synchronous reset.
CLKA, CLKB	Input	1-bit	Port A/B clock input.

Design Entry Method

This design element can be used in schematics.

This element can be inferred by most synthesis tools by properly describing the RAM behavior in standard RTL code (consult synthesis tool documentation for details). Alternatively, CORE Generator can also create the desired macro for this RAM. If it is desired to have more control over the implementation or placement of this component, it may also be directly instantiated. In order to instantiate this component, use the ISE HDL Templates or instantiation template below and paste into your code. Connect all necessary inputs to the desired signals in the design. The CLKA/CLKB clock signals must be tied to an active clock for RAM operation and the SSRA/SSRB reset signals must be either tied to a logic zero or to the proper reset signal. ENA/ENB must either be tied to a logic one or a proper RAM port enable signal. Refer to the DATA_WIDTH table below for the necessary data input, data output, write enable and address connection information for each DATA_WIDTH setting as the necessary connections for these signals change based on this attribute. All other output signals can be left unconnected (open) and all unused input signals should be tied to a logic zero.

The following table shows the necessary input and output connections for the variable input ports for each DATA_WIDTH values for either Port A or Port B:

DATA_WIDTH Value	DI, DIP Connections	ADDR Connections	WE Connections	DO, DOP Connections
1	DI[0]	ADDR[13:0]	Connect WE[3:0] to single user WE signal	DO[0]
2	DI[1:0]	ADDR[13:1]	Connect WE[3:0] to single user WE signal	DO[1:0]
4	DI[3:0]	ADDR[13:2]	Connect WE[3:0] to single user WE signal	DO[3:0]
9	DI[7:0], DIP[0]	ADDR[13:3]	Connect WE[3:0] to single user WE signal	DO[7:0], DOP[0]
18	DI[15:0], DIP[1:0]	ADDR[13:4]	Connect WE[0] and WE[2] to user WE[0] and WE[1] and WE[3] to user WE[1]	DO[15:0], DOP[1:0]
36	DI[31:0], DIP[3:0]	ADDR[13:5]	Connect each WE[3:0] signal to the associated byte write enable.	DO[31:0], DOP[3:0]

Alternatively, the prior RAMB16_Sm_Sn design elements can be instantiated if a byte-enable operation is not necessary. Also new convenience macros called RAMB16BWE_Sm_Sn are provided to allow for easier instantiation of this RAM with byte-enable operation. If either of these components is used, the software automatically re-target them to a properly configured RAMB16BWE component.

Available Attributes

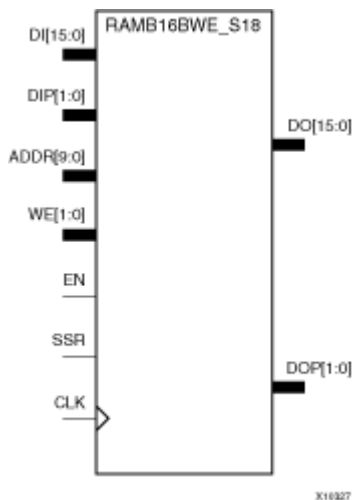
Attribute	Type	Allowed Values	Default	Description
DATA_WIDTH_A, DATA_WIDTH_B	Integer	0, 1, 2, 4, 9, 18, or 36	0	Specifies the configurable data width for Ports A and B.
INIT_A, INIT_B	Hexadecimal	Any 36-Bit Value	All zeros	Specifies the initial value on the Port B output after configuration.
SIM_COLLISION_CHECK	String	ALL, "WARNING_ONLY", "GENERATE_X_ONLY", or "NONE"	"ALL"	<p>Allows modification of the simulation behavior so that if a memory collision occurs:</p> <p>"ALL" = warning produced and affected outputs/memory location go unknown (X).</p> <p>WARNING_ONLY = warning produced and affected outputs/memory retain last value.</p> <p>GENERATE_X_ONLY = no warning, however, affected outputs/memory go unknown (X).</p> <p>NONE = no warning and affected outputs/memory retain last value.</p> <p><i>Note:</i> Setting this to a value other than "ALL" can allow problems in the design to go unnoticed during simulation. Care should be taken when changing the value of this attribute.</p>
SRVAL_A, SRVAL_B	Hexadecimal	Any 36-Bit Value	All zeros	Specifies the output value of Port B upon the assertion of the synchronous reset (SSRB) signal.
WRITE_MODE_A, WRITE_MODE_B	String	"WRITE_FIRST", "READ_FIRST", or "NO_CHANGE"	"WRITE_FIRST"	<p>Specifies output behavior of the port being written to:</p> <p>WRITE_FIRST = written value appears on output port of the RAM.</p> <p>READ_FIRST = previous RAM contents for that memory location appear on the output port.</p> <p>NO_CHANGE = previous value on the output port remains the same.</p>
INIT_00 to INIT_3F	Hexadecimal	Any 256-Bit Value	All zeros	Allows specification of the initial contents of the 16Kb data memory array.
INITP_00 to INITP_07	Hexadecimal	Any 256-Bit Value	All zeros	Allows specification of the initial contents of the 2Kb parity data memory array.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

RAMB16BWE_S18

Primitive: 16K-bit Data and 2K-bit Parity Synchronous Single Port Block RAM with 18-bit Port



Introduction

This design element can be configured and used as a 1-bit wide by 16K deep to a 36-bit wide by 512 deep single-port or dual port RAM. Both read and write operations are fully synchronous to the supplied clock(s) to the component however Port A and Port B may operate fully independent and asynchronous to each other accessing the same memory array. When configured in the wider data width modes, byte-enable write operations are possible. This Block RAM memory offers fast and flexible storage of large amounts of on-chip data.

Port Descriptions

Name	Direction	Width (Bits)	Function
DOA, DOB	Output	32-bits	Port A/B data output bus.
DOPA, DOPB	Output	4-bits	Port A/B parity output bus.
DIA, DIB	Input	32-bits	Port A/B data input bus.
DIPA, DIPB	Input	4-bits	Port A/B parity input bus.
ADDRA[13:5], ADDR[B]13:5]	Input	14-bits	Port A/B address input bus. LSB always exists on ADDRA/B[0] while the MSB is determined by the settings for DATA_WIDTH_A/B.
WEA[0:0], WEB[0:0]	Input	4-bits	Port A/B byte-wide write enable.
ENA, ENB	Input	1-bit	Port A/B enable
SSRA, SSRB	Input	1-bit	Port A/B output registers synchronous reset.
CLKA, CLKB	Input	1-bit	Port A/B clock input.

Design Entry Method

This design element can be used in schematics.

This element can be inferred by most synthesis tools by properly describing the RAM behavior in standard RTL code (consult synthesis tool documentation for details). Alternatively, CORE Generator can also create the desired macro for this RAM. If it is desired to have more control over the implementation or placement of this component, it may also be directly instantiated. In order to instantiate this component, use the ISE HDL Templates or instantiation template below and paste into your code. Connect all necessary inputs to the desired signals in the design. The CLKA/CLKB clock signals must be tied to an active clock for RAM operation and the SSRA/SSRB reset signals must be either tied to a logic zero or to the proper reset signal. ENA/ENB must either be tied to a logic one or a proper RAM port enable signal. Refer to the DATA_WIDTH table below for the necessary data input, data output, write enable and address connection information for each DATA_WIDTH setting as the necessary connections for these signals change based on this attribute. All other output signals can be left unconnected (open) and all unused input signals should be tied to a logic zero.

The following table shows the necessary input and output connections for the variable input ports for each DATA_WIDTH values for either Port A or Port B:

DATA_WIDTH Value	DI, DIP Connections	ADDR Connections	WE Connections	DO, DOP Connections
1	DI[0]	ADDR[13:0]	Connect WE[3:0] to single user WE signal	DO[0]
2	DI[1:0]	ADDR[13:1]	Connect WE[3:0] to single user WE signal	DO[1:0]
4	DI[3:0]	ADDR[13:2]	Connect WE[3:0] to single user WE signal	DO[3:0]
9	DI[7:0], DIP[0]	ADDR[13:3]	Connect WE[3:0] to single user WE signal	DO[7:0], DOP[0]
18	DI[15:0], DIP[1:0]	ADDR[13:4]	Connect WE[0] and WE[2] to user WE[0] and WE[1] and WE[3] to user WE[1]	DO[15:0], DOP[1:0]
36	DI[31:0], DIP[3:0]	ADDR[13:5]	Connect each WE[3:0] signal to the associated byte write enable.	DO[31:0], DOP[3:0]

Alternatively, the prior RAMB16_Sm_Sn design elements can be instantiated if a byte-enable operation is not necessary. Also new convenience macros called RAMB16BWE_Sm_Sn are provided to allow for easier instantiation of this RAM with byte-enable operation. If either of these components is used, the software automatically re-target them to a properly configured RAMB16BWE component.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DATA_WIDTH_A, DATA_WIDTH_B	Integer	0, 1, 2, 4, 9, 18, or 36	0	Specifies the configurable data width for Ports A and B.
INIT_A, INIT_B	Hexadecimal	Any 36-Bit Value	All zeros	Specifies the initial value on the Port B output after configuration.

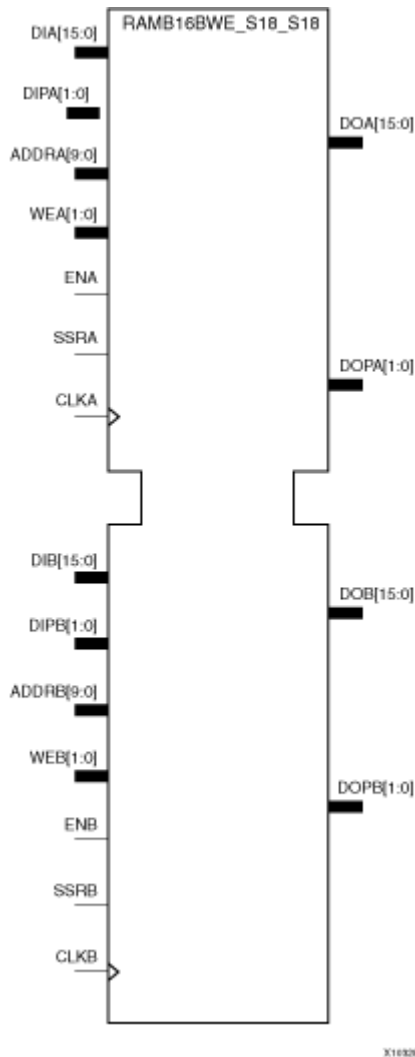
Attribute	Type	Allowed Values	Default	Description
SIM_COLLISION_CHECK	String	ALL, "WARNING_ONLY", "GENERATE_X_ONLY", or "NONE"	"ALL"	<p>Allows modification of the simulation behavior so that if a memory collision occurs:</p> <p>"ALL" = warning produced and affected outputs/memory location go unknown (X).</p> <p>WARNING_ONLY = warning produced and affected outputs/memory retain last value.</p> <p>GENERATE_X_ONLY = no warning, however, affected outputs/memory go unknown (X).</p> <p>NONE = no warning and affected outputs/memory retain last value.</p> <p><i>Note:</i> Setting this to a value other than "ALL" can allow problems in the design to go unnoticed during simulation. Care should be taken when changing the value of this attribute.</p>
SRVAL_A, SRVAL_B	Hexadecimal	Any 36-Bit Value	All zeros	Specifies the output value of Port B upon the assertion of the synchronous reset (SSRB) signal.
WRITE_MODE_A, WRITE_MODE_B	String	"WRITE_FIRST", "READ_FIRST", or "NO_CHANGE"	"WRITE_FIRST"	<p>Specifies output behavior of the port being written to:</p> <p>WRITE_FIRST = written value appears on output port of the RAM.</p> <p>READ_FIRST = previous RAM contents for that memory location appear on the output port.</p> <p>NO_CHANGE = previous value on the output port remains the same.</p>
INIT_00 to INIT_3F	Hexadecimal	Any 256-Bit Value	All zeros	Allows specification of the initial contents of the 16Kb data memory array.
INITP_00 to INITP_07	Hexadecimal	Any 256-Bit Value	All zeros	Allows specification of the initial contents of the 2Kb parity data memory array.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

RAMB16BWE_S18_S18

Primitive: 16K-bit Data and 2K-bit Parity Synchronous Dual Port Block RAM with 18-bit Ports



Introduction

This design element can be configured and used as a 1-bit wide by 16K deep to a 36-bit wide by 512 deep single-port or dual port RAM. Both read and write operations are fully synchronous to the supplied clock(s) to the component however Port A and Port B may operate fully independent and asynchronous to each other accessing the same memory array. When configured in the wider data width modes, byte-enable write operations are possible. This Block RAM memory offers fast and flexible storage of large amounts of on-chip data.

Port Descriptions

Name	Direction	Width (Bits)	Function
DOA, DOB	Output	32-bits	Port A/B data output bus.
DOPA, DOPB	Output	4-bits	Port A/B parity output bus.
DIA, DIB	Input	32-bits	Port A/B data input bus.
DIPA, DIPB	Input	4-bits	Port A/B parity input bus.

Name	Direction	Width (Bits)	Function
ADDRA[13:5], ADDR[13:5]	Input	14-bits	Port A/B address input bus. LSB always exists on ADDRA/B[0] while the MSB is determined by the settings for DATA_WIDTH_A/B.
WEA[0:0], WEB[0:0]	Input	4-bits	Port A/B byte-wide write enable.
ENA, ENB	Input	1-bit	Port A/B enable
SSRA, SSRB	Input	1-bit	Port A/B output registers synchronous reset.
CLKA, CLKB	Input	1-bit	Port A/B clock input.

Design Entry Method

This design element can be used in schematics.

This element can be inferred by most synthesis tools by properly describing the RAM behavior in standard RTL code (consult synthesis tool documentation for details). Alternatively, CORE Generator can also create the desired macro for this RAM. If it is desired to have more control over the implementation or placement of this component, it may also be directly instantiated. In order to instantiate this component, use the ISE HDL Templates or instantiation template below and paste into your code. Connect all necessary inputs to the desired signals in the design. The CLKA/CLKB clock signals must be tied to an active clock for RAM operation and the SSRA/SSRB reset signals must be either tied to a logic zero or to the proper reset signal. ENA/ENB must either be tied to a logic one or a proper RAM port enable signal. Refer to the DATA_WIDTH table below for the necessary data input, data output, write enable and address connection information for each DATA_WIDTH setting as the necessary connections for these signals change based on this attribute. All other output signals can be left unconnected (open) and all unused input signals should be tied to a logic zero.

The following table shows the necessary input and output connections for the variable input ports for each DATA_WIDTH values for either Port A or Port B:

DATA_WIDTH Value	DI, DIP Connections	ADDR Connections	WE Connections	DO, DOP Connections
1	DI[0]	ADDR[13:0]	Connect WE[3:0] to single user WE signal	DO[0]
2	DI[1:0]	ADDR[13:1]	Connect WE[3:0] to single user WE signal	DO[1:0]
4	DI[3:0]	ADDR[13:2]	Connect WE[3:0] to single user WE signal	DO[3:0]
9	DI[7:0], DIP[0]	ADDR[13:3]	Connect WE[3:0] to single user WE signal	DO[7:0], DOP[0]
18	DI[15:0], DIP[1:0]	ADDR[13:4]	Connect WE[0] and WE[2] to user WE[0] and WE[1] and WE[3] to user WE[1]	DO[15:0], DOP[1:0]
36	DI[31:0], DIP[3:0]	ADDR[13:5]	Connect each WE[3:0] signal to the associated byte write enable.	DO[31:0], DOP[3:0]

Alternatively, the prior RAMB16_Sm_Sn design elements can be instantiated if a byte-enable operation is not necessary. Also new convenience macros called RAMB16BWE_Sm_Sn are provided to allow for easier instantiation of this RAM with byte-enable operation. If either of these components is used, the software automatically re-target them to a properly configured RAMB16BWE component.

Available Attributes

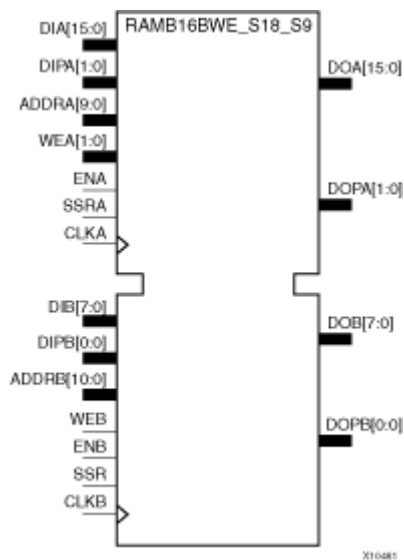
Attribute	Type	Allowed Values	Default	Description
DATA_WIDTH_A, DATA_WIDTH_B	Integer	0, 1, 2, 4, 9, 18, or 36	0	Specifies the configurable data width for Ports A and B.
INIT_A, INIT_B	Hexadecimal	Any 36-Bit Value	All zeros	Specifies the initial value on the Port B output after configuration.
SIM_COLLISION_CHECK	String	ALL, "WARNING_ONLY", "GENERATE_X_ONLY", or "NONE"	"ALL"	<p>Allows modification of the simulation behavior so that if a memory collision occurs:</p> <p>"ALL" = warning produced and affected outputs/memory location go unknown (X).</p> <p>WARNING_ONLY = warning produced and affected outputs/memory retain last value.</p> <p>GENERATE_X_ONLY = no warning, however, affected outputs/memory go unknown (X).</p> <p>NONE = no warning and affected outputs/memory retain last value.</p> <p><i>Note:</i> Setting this to a value other than "ALL" can allow problems in the design to go unnoticed during simulation. Care should be taken when changing the value of this attribute.</p>
SRVAL_A, SRVAL_B	Hexadecimal	Any 36-Bit Value	All zeros	Specifies the output value of Port B upon the assertion of the synchronous reset (SSRB) signal.
WRITE_MODE_A, WRITE_MODE_B	String	"WRITE_FIRST", "READ_FIRST", or "NO_CHANGE"	"WRITE_FIRST"	<p>Specifies output behavior of the port being written to:</p> <p>WRITE_FIRST = written value appears on output port of the RAM.</p> <p>READ_FIRST = previous RAM contents for that memory location appear on the output port.</p> <p>NO_CHANGE = previous value on the output port remains the same.</p>
INIT_00 to INIT_3F	Hexadecimal	Any 256-Bit Value	All zeros	Allows specification of the initial contents of the 16Kb data memory array.
INITP_00 to INITP_07	Hexadecimal	Any 256-Bit Value	All zeros	Allows specification of the initial contents of the 2Kb parity data memory array.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

RAMB16BWE_S18_S9

Primitive: 16K-bit Data and 2K-bit Parity Synchronous Dual Port Block RAM with 18-bit and 9-bit Ports



Introduction

This design element can be configured and used as a 1-bit wide by 16K deep to a 36-bit wide by 512 deep single-port or dual port RAM. Both read and write operations are fully synchronous to the supplied clock(s) to the component however Port A and Port B may operate fully independent and asynchronous to each other accessing the same memory array. When configured in the wider data width modes, byte-enable write operations are possible. This Block RAM memory offers fast and flexible storage of large amounts of on-chip data.

Port Descriptions

Name	Direction	Width (Bits)	Function
DOA, DOB	Output	32-bits	Port A/B data output bus.
DOPA, DOPB	Output	4-bits	Port A/B parity output bus.
DIA, DIB	Input	32-bits	Port A/B data input bus.
DIPA, DIPB	Input	4-bits	Port A/B parity input bus.
ADDRA[13:5], ADDRBE[13:5]	Input	14-bits	Port A/B address input bus. LSB always exists on ADDRA/B[0] while the MSB is determined by the settings for DATA_WIDTH_A/B.
WEA[0:0], WEB[0:0]	Input	4-bits	Port A/B byte-wide write enable.
ENA, ENB	Input	1-bit	Port A/B enable
SSRA, SSRB	Input	1-bit	Port A/B output registers synchronous reset.
CLKA, CLKB	Input	1-bit	Port A/B clock input.

Design Entry Method

This design element can be used in schematics.

This element can be inferred by most synthesis tools by properly describing the RAM behavior in standard RTL code (consult synthesis tool documentation for details). Alternatively, CORE Generator can also create the desired macro for this RAM. If it is desired to have more control over the implementation or placement of this component, it may also be directly instantiated. In order to instantiate this component, use the ISE HDL Templates or instantiation template below and paste into your code. Connect all necessary inputs to the desired signals in the design. The CLKA/CLKB clock signals must be tied to an active clock for RAM operation and the SSRA/SSRB reset signals must be either tied to a logic zero or to the proper reset signal. ENA/ENB must either be tied to a logic one or a proper RAM port enable signal. Refer to the DATA_WIDTH table below for the necessary data input, data output, write enable and address connection information for each DATA_WIDTH setting as the necessary connections for these signals change based on this attribute. All other output signals can be left unconnected (open) and all unused input signals should be tied to a logic zero.

The following table shows the necessary input and output connections for the variable input ports for each DATA_WIDTH values for either Port A or Port B:

DATA_WIDTH Value	DI, DIP Connections	ADDR Connections	WE Connections	DO, DOP Connections
1	DI[0]	ADDR[13:0]	Connect WE[3:0] to single user WE signal	DO[0]
2	DI[1:0]	ADDR[13:1]	Connect WE[3:0] to single user WE signal	DO[1:0]
4	DI[3:0]	ADDR[13:2]	Connect WE[3:0] to single user WE signal	DO[3:0]
9	DI[7:0], DIP[0]	ADDR[13:3]	Connect WE[3:0] to single user WE signal	DO[7:0], DOP[0]
18	DI[15:0], DIP[1:0]	ADDR[13:4]	Connect WE[0] and WE[2] to user WE[0] and WE[1] and WE[3] to user WE[1]	DO[15:0], DOP[1:0]
36	DI[31:0], DIP[3:0]	ADDR[13:5]	Connect each WE[3:0] signal to the associated byte write enable.	DO[31:0], DOP[3:0]

Alternatively, the prior RAMB16_Sm_Sn design elements can be instantiated if a byte-enable operation is not necessary. Also new convenience macros called RAMB16BWE_Sm_Sn are provided to allow for easier instantiation of this RAM with byte-enable operation. If either of these components is used, the software automatically re-target them to a properly configured RAMB16BWE component.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DATA_WIDTH_A, DATA_WIDTH_B	Integer	0, 1, 2, 4, 9, 18, or 36	0	Specifies the configurable data width for Ports A and B.
INIT_A, INIT_B	Hexadecimal	Any 36-Bit Value	All zeros	Specifies the initial value on the Port B output after configuration.

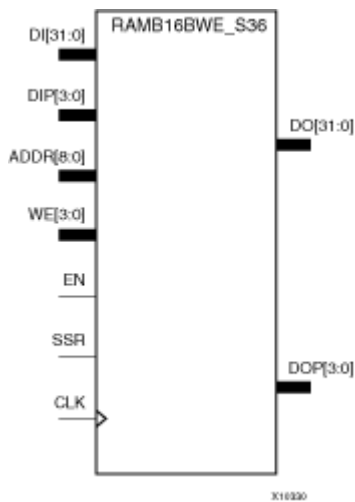
Attribute	Type	Allowed Values	Default	Description
SIM_COLLISION_CHECK	String	ALL, "WARNING_ONLY", "GENERATE_X_ONLY", or "NONE"	"ALL"	<p>Allows modification of the simulation behavior so that if a memory collision occurs:</p> <p>"ALL" = warning produced and affected outputs/memory location go unknown (X).</p> <p>WARNING_ONLY = warning produced and affected outputs/memory retain last value.</p> <p>GENERATE_X_ONLY = no warning, however, affected outputs/memory go unknown (X).</p> <p>NONE = no warning and affected outputs/memory retain last value.</p> <p><i>Note:</i> Setting this to a value other than "ALL" can allow problems in the design to go unnoticed during simulation. Care should be taken when changing the value of this attribute.</p>
SRVAL_A, SRVAL_B	Hexadecimal	Any 36-Bit Value	All zeros	Specifies the output value of Port B upon the assertion of the synchronous reset (SSRB) signal.
WRITE_MODE_A, WRITE_MODE_B	String	"WRITE_FIRST", "READ_FIRST", or "NO_CHANGE"	"WRITE_FIRST"	<p>Specifies output behavior of the port being written to:</p> <p>WRITE_FIRST = written value appears on output port of the RAM.</p> <p>READ_FIRST = previous RAM contents for that memory location appear on the output port.</p> <p>NO_CHANGE = previous value on the output port remains the same.</p>
INIT_00 to INIT_3F	Hexadecimal	Any 256-Bit Value	All zeros	Allows specification of the initial contents of the 16Kb data memory array.
INITP_00 to INITP_07	Hexadecimal	Any 256-Bit Value	All zeros	Allows specification of the initial contents of the 2Kb parity data memory array.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

RAMB16BWE_S36

Primitive: 16K-bit Data and 2K-bit Parity Synchronous Single Port Block RAM with 36-Bit Port



Introduction

This design element can be configured and used as a 1-bit wide by 16K deep to a 36-bit wide by 512 deep single-port or dual port RAM. Both read and write operations are fully synchronous to the supplied clock(s) to the component however Port A and Port B may operate fully independent and asynchronous to each other accessing the same memory array. When configured in the wider data width modes, byte-enable write operations are possible. This Block RAM memory offers fast and flexible storage of large amounts of on-chip data.

Port Descriptions

Name	Direction	Width (Bits)	Function
DOA, DOB	Output	32-bits	Port A/B data output bus.
DOPA, DOPB	Output	4-bits	Port A/B parity output bus.
DIA, DIB	Input	32-bits	Port A/B data input bus.
DIPA, DIPB	Input	4-bits	Port A/B parity input bus.
ADDRA[13:5], ADDR[B]13:5]	Input	14-bits	Port A/B address input bus. LSB always exists on ADDRA/B[0] while the MSB is determined by the settings for DATA_WIDTH_A/B.
WEA[0:0], WEB[0:0]	Input	4-bits	Port A/B byte-wide write enable.
ENA, ENB	Input	1-bit	Port A/B enable
SSRA, SSRB	Input	1-bit	Port A/B output registers synchronous reset.
CLKA, CLKB	Input	1-bit	Port A/B clock input.

Design Entry Method

This design element can be used in schematics.

This element can be inferred by most synthesis tools by properly describing the RAM behavior in standard RTL code (consult synthesis tool documentation for details). Alternatively, CORE Generator can also create the desired macro for this RAM. If it is desired to have more control over the implementation or placement of this component, it may also be directly instantiated. In order to instantiate this component, use the ISE HDL Templates or instantiation template below and paste into your code. Connect all necessary inputs to the desired signals in the design. The CLKA/CLKB clock signals must be tied to an active clock for RAM operation and the SSRA/SSRB reset signals must be either tied to a logic zero or to the proper reset signal. ENA/ENB must either be tied to a logic one or a proper RAM port enable signal. Refer to the DATA_WIDTH table below for the necessary data input, data output, write enable and address connection information for each DATA_WIDTH setting as the necessary connections for these signals change based on this attribute. All other output signals can be left unconnected (open) and all unused input signals should be tied to a logic zero.

The following table shows the necessary input and output connections for the variable input ports for each DATA_WIDTH values for either Port A or Port B:

DATA_WIDTH Value	DI, DIP Connections	ADDR Connections	WE Connections	DO, DOP Connections
1	DI[0]	ADDR[13:0]	Connect WE[3:0] to single user WE signal	DO[0]
2	DI[1:0]	ADDR[13:1]	Connect WE[3:0] to single user WE signal	DO[1:0]
4	DI[3:0]	ADDR[13:2]	Connect WE[3:0] to single user WE signal	DO[3:0]
9	DI[7:0], DIP[0]	ADDR[13:3]	Connect WE[3:0] to single user WE signal	DO[7:0], DOP[0]
18	DI[15:0], DIP[1:0]	ADDR[13:4]	Connect WE[0] and WE[2] to user WE[0] and WE[1] and WE[3] to user WE[1]	DO[15:0], DOP[1:0]
36	DI[31:0], DIP[3:0]	ADDR[13:5]	Connect each WE[3:0] signal to the associated byte write enable.	DO[31:0], DOP[3:0]

Alternatively, the prior RAMB16_Sm_Sn design elements can be instantiated if a byte-enable operation is not necessary. Also new convenience macros called RAMB16BWE_Sm_Sn are provided to allow for easier instantiation of this RAM with byte-enable operation. If either of these components is used, the software automatically re-target them to a properly configured RAMB16BWE component.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DATA_WIDTH_A, DATA_WIDTH_B	Integer	0, 1, 2, 4, 9, 18, or 36	0	Specifies the configurable data width for Ports A and B.
INIT_A, INIT_B	Hexadecimal	Any 36-Bit Value	All zeros	Specifies the initial value on the Port B output after configuration.

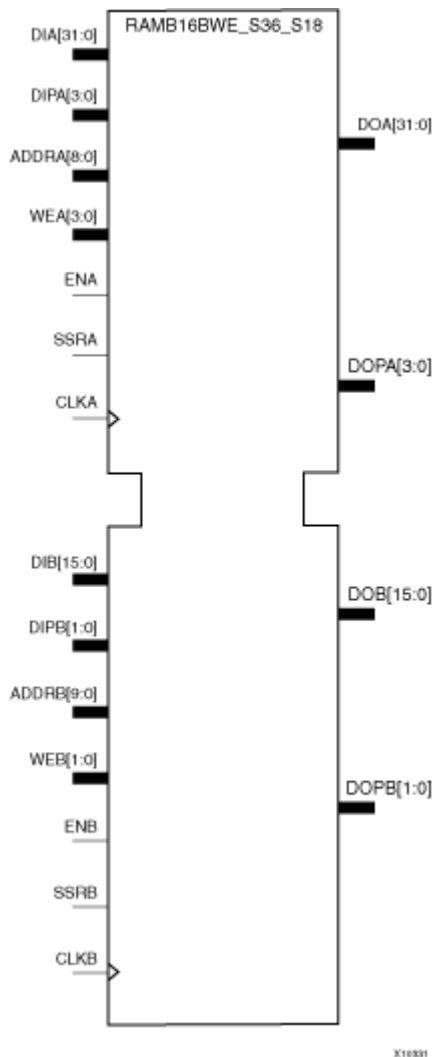
Attribute	Type	Allowed Values	Default	Description
SIM_COLLISION_CHECK	String	ALL, "WARNING_ONLY", "GENERATE_X_ONLY", or "NONE"	"ALL"	<p>Allows modification of the simulation behavior so that if a memory collision occurs:</p> <p>"ALL" = warning produced and affected outputs/memory location go unknown (X).</p> <p>WARNING_ONLY = warning produced and affected outputs/memory retain last value.</p> <p>GENERATE_X_ONLY = no warning, however, affected outputs/memory go unknown (X).</p> <p>NONE = no warning and affected outputs/memory retain last value.</p> <p><i>Note:</i> Setting this to a value other than "ALL" can allow problems in the design to go unnoticed during simulation. Care should be taken when changing the value of this attribute.</p>
SRVAL_A, SRVAL_B	Hexadecimal	Any 36-Bit Value	All zeros	Specifies the output value of Port B upon the assertion of the synchronous reset (SSRB) signal.
WRITE_MODE_A, WRITE_MODE_B	String	"WRITE_FIRST", "READ_FIRST", or "NO_CHANGE"	"WRITE_FIRST"	<p>Specifies output behavior of the port being written to:</p> <p>WRITE_FIRST = written value appears on output port of the RAM.</p> <p>READ_FIRST = previous RAM contents for that memory location appear on the output port.</p> <p>NO_CHANGE = previous value on the output port remains the same.</p>
INIT_00 to INIT_3F	Hexadecimal	Any 256-Bit Value	All zeros	Allows specification of the initial contents of the 16Kb data memory array.
INITP_00 to INITP_07	Hexadecimal	Any 256-Bit Value	All zeros	Allows specification of the initial contents of the 2Kb parity data memory array.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

RAMB16BWE_S36_S18

Primitive: 16K-bit Data and 2K-bit Parity Synchronous Dual Port Block RAM with 36-bit and 18-bit Ports



Introduction

This design element can be configured and used as a 1-bit wide by 16K deep to a 36-bit wide by 512 deep single-port or dual port RAM. Both read and write operations are fully synchronous to the supplied clock(s) to the component however Port A and Port B may operate fully independent and asynchronous to each other accessing the same memory array. When configured in the wider data width modes, byte-enable write operations are possible. This Block RAM memory offers fast and flexible storage of large amounts of on-chip data.

Port Descriptions

Name	Direction	Width (Bits)	Function
DOA, DOB	Output	32-bits	Port A/B data output bus.
DOPA, DOPB	Output	4-bits	Port A/B parity output bus.
DIA, DIB	Input	32-bits	Port A/B data input bus.

Name	Direction	Width (Bits)	Function
DIPA, DIPB	Input	4-bits	Port A/B parity input bus.
ADDRA[13:5], ADDR[13:5]	Input	14-bits	Port A/B address input bus. LSB always exists on ADDRA/B[0] while the MSB is determined by the settings for DATA_WIDTH_A/B.
WEA[0:0], WEB[0:0]	Input	4-bits	Port A/B byte-wide write enable.
ENA, ENB	Input	1-bit	Port A/B enable
SSRA, SSRB	Input	1-bit	Port A/B output registers synchronous reset.
CLKA, CLKB	Input	1-bit	Port A/B clock input.

Design Entry Method

This design element can be used in schematics.

This element can be inferred by most synthesis tools by properly describing the RAM behavior in standard RTL code (consult synthesis tool documentation for details). Alternatively, CORE Generator can also create the desired macro for this RAM. If it is desired to have more control over the implementation or placement of this component, it may also be directly instantiated. In order to instantiate this component, use the ISE HDL Templates or instantiation template below and paste into your code. Connect all necessary inputs to the desired signals in the design. The CLKA/CLKB clock signals must be tied to an active clock for RAM operation and the SSRA/SSRB reset signals must be either tied to a logic zero or to the proper reset signal. ENA/ENB must either be tied to a logic one or a proper RAM port enable signal. Refer to the DATA_WIDTH table below for the necessary data input, data output, write enable and address connection information for each DATA_WIDTH setting as the necessary connections for these signals change based on this attribute. All other output signals can be left unconnected (open) and all unused input signals should be tied to a logic zero.

The following table shows the necessary input and output connections for the variable input ports for each DATA_WIDTH values for either Port A or Port B:

DATA_WIDTH Value	DI, DIP Connections	ADDR Connections	WE Connections	DO, DOP Connections
1	DI[0]	ADDR[13:0]	Connect WE[3:0] to single user WE signal	DO[0]
2	DI[1:0]	ADDR[13:1]	Connect WE[3:0] to single user WE signal	DO[1:0]
4	DI[3:0]	ADDR[13:2]	Connect WE[3:0] to single user WE signal	DO[3:0]
9	DI[7:0], DIP[0]	ADDR[13:3]	Connect WE[3:0] to single user WE signal	DO[7:0], DOP[0]
18	DI[15:0], DIP[1:0]	ADDR[13:4]	Connect WE[0] and WE[2] to user WE[0] and WE[1] and WE[3] to user WE[1]	DO[15:0], DOP[1:0]
36	DI[31:0], DIP[3:0]	ADDR[13:5]	Connect each WE[3:0] signal to the associated byte write enable.	DO[31:0], DOP[3:0]

Alternatively, the prior RAMB16_Sm_Sn design elements can be instantiated if a byte-enable operation is not necessary. Also new convenience macros called RAMB16BWE_Sm_Sn are provided to allow for easier instantiation of this RAM with byte-enable operation. If either of these components is used, the software automatically re-target them to a properly configured RAMB16BWE component.

Available Attributes

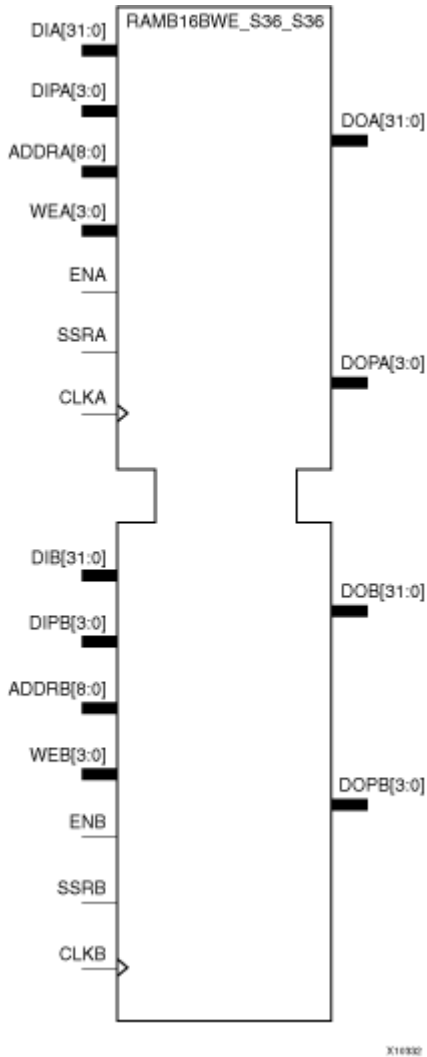
Attribute	Type	Allowed Values	Default	Description
DATA_WIDTH_A, DATA_WIDTH_B	Integer	0, 1, 2, 4, 9, 18, or 36	0	Specifies the configurable data width for Ports A and B.
INIT_A, INIT_B	Hexadecimal	Any 36-Bit Value	All zeros	Specifies the initial value on the Port B output after configuration.
SIM_COLLISION_CHECK	String	ALL, "WARNING_ONLY", "GENERATE_X_ONLY", or "NONE"	"ALL"	<p>Allows modification of the simulation behavior so that if a memory collision occurs:</p> <p>"ALL" = warning produced and affected outputs/memory location go unknown (X).</p> <p>WARNING_ONLY = warning produced and affected outputs/memory retain last value.</p> <p>GENERATE_X_ONLY = no warning, however, affected outputs/memory go unknown (X).</p> <p>NONE = no warning and affected outputs/memory retain last value.</p> <p><i>Note:</i> Setting this to a value other than "ALL" can allow problems in the design to go unnoticed during simulation. Care should be taken when changing the value of this attribute.</p>
SRVAL_A, SRVAL_B	Hexadecimal	Any 36-Bit Value	All zeros	Specifies the output value of Port B upon the assertion of the synchronous reset (SSRB) signal.
WRITE_MODE_A, WRITE_MODE_B	String	"WRITE_FIRST", "READ_FIRST", or "NO_CHANGE"	"WRITE_FIRST"	<p>Specifies output behavior of the port being written to:</p> <p>WRITE_FIRST = written value appears on output port of the RAM.</p> <p>READ_FIRST = previous RAM contents for that memory location appear on the output port.</p> <p>NO_CHANGE = previous value on the output port remains the same.</p>
INIT_00 to INIT_3F	Hexadecimal	Any 256-Bit Value	All zeros	Allows specification of the initial contents of the 16Kb data memory array.
INITP_00 to INITP_07	Hexadecimal	Any 256-Bit Value	All zeros	Allows specification of the initial contents of the 2Kb parity data memory array.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

RAMB16BWE_S36_S36

Primitive: 16K-bit Data and 2K-bit Parity Synchronous Dual Port Block RAM with 36-bit Ports



Introduction

This design element can be configured and used as a 1-bit wide by 16K deep to a 36-bit wide by 512 deep single-port or dual port RAM. Both read and write operations are fully synchronous to the supplied clock(s) to the component however Port A and Port B may operate fully independent and asynchronous to each other accessing the same memory array. When configured in the wider data width modes, byte-enable write operations are possible. This Block RAM memory offers fast and flexible storage of large amounts of on-chip data.

Port Descriptions

Name	Direction	Width (Bits)	Function
DOA, DOB	Output	32-bits	Port A/B data output bus.
DOPA, DOPB	Output	4-bits	Port A/B parity output bus.
DIA, DIB	Input	32-bits	Port A/B data input bus.
DIPA, DIPB	Input	4-bits	Port A/B parity input bus.

Name	Direction	Width (Bits)	Function
ADDRA[13:5], ADDR[13:5]	Input	14-bits	Port A/B address input bus. LSB always exists on ADDRA/B[0] while the MSB is determined by the settings for DATA_WIDTH_A/B.
WEA[0:0], WEB[0:0]	Input	4-bits	Port A/B byte-wide write enable.
ENA, ENB	Input	1-bit	Port A/B enable
SSRA, SSRB	Input	1-bit	Port A/B output registers synchronous reset.
CLKA, CLKB	Input	1-bit	Port A/B clock input.

Design Entry Method

This design element can be used in schematics.

This element can be inferred by most synthesis tools by properly describing the RAM behavior in standard RTL code (consult synthesis tool documentation for details). Alternatively, CORE Generator can also create the desired macro for this RAM. If it is desired to have more control over the implementation or placement of this component, it may also be directly instantiated. In order to instantiate this component, use the ISE HDL Templates or instantiation template below and paste into your code. Connect all necessary inputs to the desired signals in the design. The CLKA/CLKB clock signals must be tied to an active clock for RAM operation and the SSRA/SSRB reset signals must be either tied to a logic zero or to the proper reset signal. ENA/ENB must either be tied to a logic one or a proper RAM port enable signal. Refer to the DATA_WIDTH table below for the necessary data input, data output, write enable and address connection information for each DATA_WIDTH setting as the necessary connections for these signals change based on this attribute. All other output signals can be left unconnected (open) and all unused input signals should be tied to a logic zero.

The following table shows the necessary input and output connections for the variable input ports for each DATA_WIDTH values for either Port A or Port B:

DATA_WIDTH Value	DI, DIP Connections	ADDR Connections	WE Connections	DO, DOP Connections
1	DI[0]	ADDR[13:0]	Connect WE[3:0] to single user WE signal	DO[0]
2	DI[1:0]	ADDR[13:1]	Connect WE[3:0] to single user WE signal	DO[1:0]
4	DI[3:0]	ADDR[13:2]	Connect WE[3:0] to single user WE signal	DO[3:0]
9	DI[7:0], DIP[0]	ADDR[13:3]	Connect WE[3:0] to single user WE signal	DO[7:0], DOP[0]
18	DI[15:0], DIP[1:0]	ADDR[13:4]	Connect WE[0] and WE[2] to user WE[0] and WE[1] and WE[3] to user WE[1]	DO[15:0], DOP[1:0]
36	DI[31:0], DIP[3:0]	ADDR[13:5]	Connect each WE[3:0] signal to the associated byte write enable.	DO[31:0], DOP[3:0]

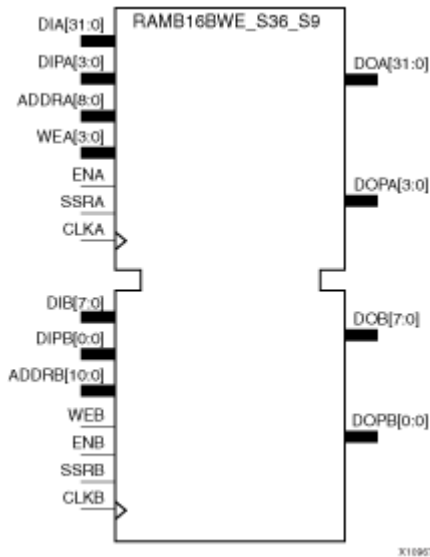
Alternatively, the prior RAMB16_Sm_Sn design elements can be instantiated if a byte-enable operation is not necessary. Also new convenience macros called RAMB16BWE_Sm_Sn are provided to allow for easier instantiation of this RAM with byte-enable operation. If either of these components is used, the software automatically re-target them to a properly configured RAMB16BWE component.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

RAMB16BWE_S36_S9

Primitive: 16K-bit Data and 2K-bit Parity Synchronous Dual Port Block RAM with 36-bit and 9-bit Ports



Introduction

This design element can be configured and used as a 1-bit wide by 16K deep to a 36-bit wide by 512 deep single-port or dual port RAM. Both read and write operations are fully synchronous to the supplied clock(s) to the component however Port A and Port B may operate fully independent and asynchronous to each other accessing the same memory array. When configured in the wider data width modes, byte-enable write operations are possible. This Block RAM memory offers fast and flexible storage of large amounts of on-chip data.

Port Descriptions

Name	Direction	Width (Bits)	Function
DOA, DOB	Output	32-bits	Port A/B data output bus.
DOPA, DOPB	Output	4-bits	Port A/B parity output bus.
DIA, DIB	Input	32-bits	Port A/B data input bus.
DIPA, DIPB	Input	4-bits	Port A/B parity input bus.
ADDRA[13:5], ADDR[B:0:0]	Input	14-bits	Port A/B address input bus. LSB always exists on ADDRA/B[0] while the MSB is determined by the settings for DATA_WIDTH_A/B.
WEA[0:0], WEB[0:0]	Input	4-bits	Port A/B byte-wide write enable.
ENA, ENB	Input	1-bit	Port A/B enable
SSRA, SSRB	Input	1-bit	Port A/B output registers synchronous reset.
CLKA, CLKB	Input	1-bit	Port A/B clock input.

Design Entry Method

This design element can be used in schematics.

This element can be inferred by most synthesis tools by properly describing the RAM behavior in standard RTL code (consult synthesis tool documentation for details). Alternatively, CORE Generator can also create the desired macro for this RAM. If it is desired to have more control over the implementation or placement of this component, it may also be directly instantiated. In order to instantiate this component, use the ISE HDL Templates or instantiation template below and paste into your code. Connect all necessary inputs to the desired signals in the design. The CLKA/CLKB clock signals must be tied to an active clock for RAM operation and the SSRA/SSRB reset signals must be either tied to a logic zero or to the proper reset signal. ENA/ENB must either be tied to a logic one or a proper RAM port enable signal. Refer to the DATA_WIDTH table below for the necessary data input, data output, write enable and address connection information for each DATA_WIDTH setting as the necessary connections for these signals change based on this attribute. All other output signals can be left unconnected (open) and all unused input signals should be tied to a logic zero.

The following table shows the necessary input and output connections for the variable input ports for each DATA_WIDTH values for either Port A or Port B:

DATA_WIDTH Value	DI, DIP Connections	ADDR Connections	WE Connections	DO, DOP Connections
1	DI[0]	ADDR[13:0]	Connect WE[3:0] to single user WE signal	DO[0]
2	DI[1:0]	ADDR[13:1]	Connect WE[3:0] to single user WE signal	DO[1:0]
4	DI[3:0]	ADDR[13:2]	Connect WE[3:0] to single user WE signal	DO[3:0]
9	DI[7:0], DIP[0]	ADDR[13:3]	Connect WE[3:0] to single user WE signal	DO[7:0], DOP[0]
18	DI[15:0], DIP[1:0]	ADDR[13:4]	Connect WE[0] and WE[2] to user WE[0] and WE[1] and WE[3] to user WE[1]	DO[15:0], DOP[1:0]
36	DI[31:0], DIP[3:0]	ADDR[13:5]	Connect each WE[3:0] signal to the associated byte write enable.	DO[31:0], DOP[3:0]

Alternatively, the prior RAMB16_Sm_Sn design elements can be instantiated if a byte-enable operation is not necessary. Also new convenience macros called RAMB16BWE_Sm_Sn are provided to allow for easier instantiation of this RAM with byte-enable operation. If either of these components is used, the software automatically re-target them to a properly configured RAMB16BWE component.

Available Attributes

Attribute	Type	Allowed Values	Default	Description
DATA_WIDTH_A, DATA_WIDTH_B	Integer	0, 1, 2, 4, 9, 18, or 36	0	Specifies the configurable data width for Ports A and B.
INIT_A, INIT_B	Hexadecimal	Any 36-Bit Value	All zeros	Specifies the initial value on the Port B output after configuration.

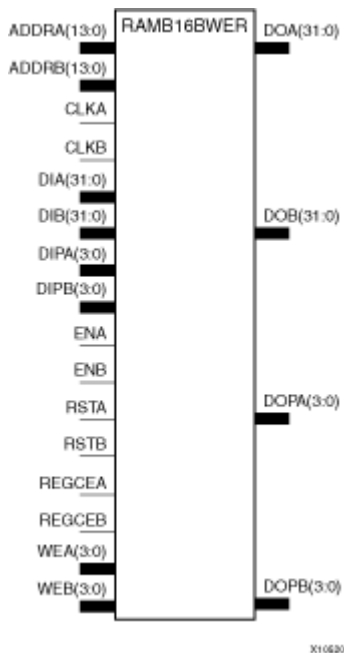
Attribute	Type	Allowed Values	Default	Description
SIM_COLLISION_CHECK	String	ALL, "WARNING_ONLY", "GENERATE_X_ONLY", or "NONE"	"ALL"	Allows modification of the simulation behavior so that if a memory collision occurs: "ALL" = warning produced and affected outputs/memory location go unknown (X). WARNING_ONLY = warning produced and affected outputs/memory retain last value. GENERATE_X_ONLY = no warning, however, affected outputs/memory go unknown (X). NONE = no warning and affected outputs/memory retain last value. <i>Note:</i> Setting this to a value other than "ALL" can allow problems in the design to go unnoticed during simulation. Care should be taken when changing the value of this attribute.
SRVAL_A, SRVAL_B	Hexadecimal	Any 36-Bit Value	All zeros	Specifies the output value of Port B upon the assertion of the synchronous reset (SSRB) signal.
WRITE_MODE_A, WRITE_MODE_B	String	"WRITE_FIRST", "READ_FIRST", or "NO_CHANGE"	"WRITE_FIRST"	Specifies output behavior of the port being written to: WRITE_FIRST = written value appears on output port of the RAM. READ_FIRST = previous RAM contents for that memory location appear on the output port. NO_CHANGE = previous value on the output port remains the same.
INIT_00 to INIT_3F	Hexadecimal	Any 256-Bit Value	All zeros	Allows specification of the initial contents of the 16Kb data memory array.
INITP_00 to INITP_07	Hexadecimal	Any 256-Bit Value	All zeros	Allows specification of the initial contents of the 2Kb parity data memory array.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

RAMB16BWER

Primitive: 16K-bit Data and 2K-bit Parity Configurable Synchronous Dual Port Block RAM with Optional Output Registers



Introduction

Note This element is available only for Spartan-3A DSP parts.

This design element contains several block RAM memories that can be configured as general-purpose 16Kb data + 2Kb parity RAM/ROM memories. These block RAM memories offer fast and flexible storage of large amounts of on-chip data. This component can be configured and used as a 1-bit wide by 16K deep to a 36-bit wide by 512 deep, single-port or dual port RAM. Both read and write operations are fully synchronous to the supplied clock(s) to the component. However, Port A and Port B can operate fully independent and asynchronous to each other, accessing the same memory array. When these ports are configured in the wider data width modes, byte-enable write operations are possible. This RAM also offers a configurable output register that can be enabled in order to improve clock-to-out times of the RAM while incurring an extra clock cycle of latency during the read operation.

Port Descriptions

The following table shows the necessary input and output connections for the variable input ports for each DATA_WIDTH values for either Port A or Port B.

DATA_WIDTH Value	DI, DIP Connections	ADDR Connections	WE Connections	DO, DOP Connections
1	DI[0]	ADDR[13:0]	Connect WE[3:0] to single user WE signal.	DO[0]
2	DI[1:0]	ADDR[13:1]	Connect WE[3:0] to single user WE signal.	DO[1:0]
4	DI[3:0]	ADDR[13:2]	Connect WE[3:0] to single user WE signal.	DO[3:0]
9	DI[7:0], DIP[0]	ADDR[13:3]	Connect WE[3:0] to single user WE signal.	DO[7:0], DOP[0]

DATA_WIDTH Value	DI, DIP Connections	ADDR Connections	WE Connections	DO, DOP Connections
18	DI[15:0], DIP[1:0]	ADDR[13:4]	Connect WE[0] and WE[2] to user WE[0] and WE[1] and WE[3] to user WE[1].	DO[15:0], DOP[1:0]
36	DI[31:0], DIP[3:0]	ADDR[13:5]	Connect each WE[3:0] signal to the associated byte write enable/.	DO[31:0], DOP[3:0]

Alternatively, the prior RAMB16_Sm_Sn and RAMB16BWER_Sm_Sn elements can be instantiated if the output registers are not necessary. If any of these components are used, the software will automatically re-target them the a properly configured RAMB16BWER element.

Name	Direction	Width (Bits)	Function
DOA, DOB	Output	32-bits	Port A/B data output bus.
DOPA, DOPB	Output	4-bits	Port A/B parity output bus.
DIA, DIB	Input	32-bits	Port A/B data input bus.
DIPA, DIPB	Input	4-bits	Port A/B parity input bus.
ADDRA, ADDR B	Input	14-bits	Port A/B address input bus. MSB always exists on ADDRA/B[13] while the LSB is determined by the settings for DATA_WIDTH_A/B.
WEA, WEB	Input	4-bits	Port A/B byte-wide write enable.
ENA, ENB	Input	1-bit	Port A/B enable.
REGCEA, REGCEB	Input	1-bit	Output register clock enable.
RSTA, RSTB	Input	1-bit	Port A/B output registers set/reset. This reset is configurable to be synchronous or asynchronous, depending on the value of the RSTTYPE attribute.
CLKA, CLKB	Input	1-bit	Port A/B clock input.

Design Entry Method

This design element can be used in schematics.

Connect all necessary inputs to the desired signals in the design. The CLKA/CLKB clock signals must be tied to an active clock for RAM operation, and the SRA/SRB reset signals must be either tied to a logic zero or to the proper reset signal. ENA/ENB must either be tied to a logic one or a proper RAM port enable signal. REGCEA and REGCEB must be tied to the proper output register clock enable, or a logic one if the respective DOA_REG or DOB_REG attribute is set to 1. If DOA_REG is set to 0, then tie REGCEA and REGCEB must be set to a logic 0.

Refer to the DATA_WIDTH column in the “Port Description” table (above) for the necessary data input, data output, write enable and address connection information for each DATA_WIDTH setting, since the necessary connections for these signals change, based on this attribute. All other output signals can be left unconnected (open) and all unused input signals should be tied to a logic zero.

Available Attributes

Attribute(s)	Type	Allowed Values	Default	Description
DATA_WIDTH_A, DATA_WIDTH_B	Integer	1, 2, 4, 9, 18, or 36	0	Specifies the configurable data width for Ports A and B.

Attribute(s)	Type	Allowed Values	Default	Description
DOA_REG, DOB_REG	Integer	0 or 1	0	Specifies to use or bypass the output registers for the RAM.
INIT_A, INIT_B	Hexadecimal	Any 36-bit Hexadecimal Value	All zeroes	Specifies the initial value on the Port B output after configuration.
SIM_COLLISION_CHECK	String	"ALL", "WARNING_ONLY", "GENERATE_X_ONLY" or "NONE"	"ALL"	<p>Allows modification of the simulation behavior so that if a memory collision occurs:</p> <p>"ALL" = warning produced and affected outputs/memory location go unknown (X).</p> <p>"WARNING_ONLY" = warning produced and affected outputs/memory retain last value.</p> <p>"GENERATE_X_ONLY" = no warning, however affected outputs/memory go unknown (X)</p> <p>"NONE" = no warning and affected outputs/memory retain last value.</p> <p><i>Note:</i> Setting this to a value other than "ALL" can allow problems in the design to go unnoticed during simulation. Care should be taken when changing the value of this attribute.</p>
SRVAL_A	Hexadecimal	Any 36-Bit Value	All zeroes	Specifies the output value of Port A upon the assertion of the reset (RSTA) signal.
SRVAL_B	Hexadecimal	Any 36-Bit Value	All zeroes	Specifies the output value of Port B upon the assertion of the reset (RSTB) signal.

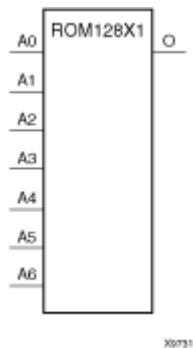
Attribute(s)	Type	Allowed Values	Default	Description
RSTTYPE	String	"ASYNC", "SYNC"	"SYNC"	Selects whether the RAM outputs should have a synchronous or asynchronous reset capability. Due to improved timing and circuit stability, it is recommended to always have this set to "SYNC" unless an asynchronous reset is absolutely necessary.
WRITE_MODE_A, WRITE_MODE_B	String	"WRITE_FIRST", "READ_FIRST", or "NO_CHANGE"	"WRITE_FIRST"	Specifies output behavior of the port being written to: "WRITE_FIRST" = written value appears on output port of the RAM. "READ_FIRST" = previous RAM contents for that memory location appear on the output port. "NO_CHANGE" = previous value on the output port remains the same.
INIT_00 to INIT_3F	Hexadecimal	Any 256-bit hexadecimal value	All zeroes	Allows specification of the initial contents of the 16Kb data memory array.
INITP_00 to INITP_07	Hexadecimal	Any 256-bit hexadecimal value	All zeroes	Allows specification of the initial contents of the 2Kb parity data memory array.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ROM128X1

Primitive: 128-Deep by 1-Wide ROM



Introduction

This design element is a 128-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 7-bit address (A6 – A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of 32 hexadecimal digits that are written into the ROM from the most-significant digit A=FH to the least-significant digit A=0H. An error occurs if the INIT=value is not specified.

Logic Table

Input				Output
I0	I1	I2	I3	O
0	0	0	0	INIT(0)
0	0	0	1	INIT(1)
0	0	1	0	INIT(2)
0	0	1	1	INIT(3)
0	1	0	0	INIT(4)
0	1	0	1	INIT(5)
0	1	1	0	INIT(6)
0	1	1	1	INIT(7)
1	0	0	0	INIT(8)
1	0	0	1	INIT(9)
1	0	1	0	INIT(10)
1	0	1	1	INIT(11)
1	1	0	0	INIT(12)
1	1	0	1	INIT(13)
1	1	1	0	INIT(14)
1	1	1	1	INIT(15)

Design Entry Method

This design element can be used in schematics.

Available Attributes

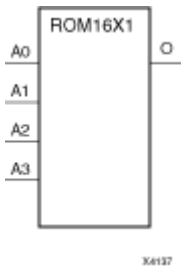
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 128-Bit Value	All zeros	Specifies the contents of the ROM.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ROM16X1

Primitive: 16-Deep by 1-Wide ROM



Introduction

This design element is a 16-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 4-bit address (A3 – A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of four hexadecimal digits that are written into the ROM from the most-significant digit A=FH to the least-significant digit A=0H. For example, the INIT=10A7 parameter produces the data stream: 0001 0000 1010 0111. An error occurs if the INIT=value is not specified.

Logic Table

Input				Output
I0	I1	I2	I3	O
0	0	0	0	INIT(0)
0	0	0	1	INIT(1)
0	0	1	0	INIT(2)
0	0	1	1	INIT(3)
0	1	0	0	INIT(4)
0	1	0	1	INIT(5)
0	1	1	0	INIT(6)
0	1	1	1	INIT(7)
1	0	0	0	INIT(8)
1	0	0	1	INIT(9)
1	0	1	0	INIT(10)
1	0	1	1	INIT(11)
1	1	0	0	INIT(12)
1	1	0	1	INIT(13)
1	1	1	0	INIT(14)
1	1	1	1	INIT(15)

Design Entry Method

This design element can be used in schematics.

Available Attributes

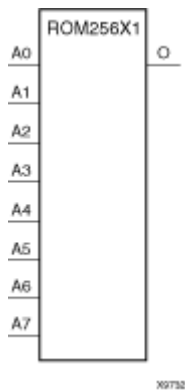
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Specifies the contents of the ROM.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ROM256X1

Primitive: 256-Deep by 1-Wide ROM



Introduction

This design element is a 256-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 8-bit address (A7– A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of 64 hexadecimal digits that are written into the ROM from the most-significant digit A=FH to the least-significant digit A=0H.

An error occurs if the INIT=value is not specified.

Logic Table

Input				Output
I0	I1	I2	I3	O
0	0	0	0	INIT(0)
0	0	0	1	INIT(1)
0	0	1	0	INIT(2)
0	0	1	1	INIT(3)
0	1	0	0	INIT(4)
0	1	0	1	INIT(5)
0	1	1	0	INIT(6)
0	1	1	1	INIT(7)
1	0	0	0	INIT(8)
1	0	0	1	INIT(9)
1	0	1	0	INIT(10)
1	0	1	1	INIT(11)
1	1	0	0	INIT(12)
1	1	0	1	INIT(13)
1	1	1	0	INIT(14)
1	1	1	1	INIT(15)

Design Entry Method

This design element can be used in schematics.

Available Attributes

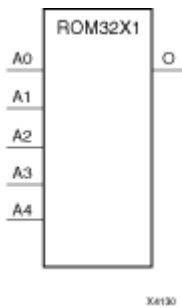
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 256-Bit Value	All zeros	Specifies the contents of the ROM.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ROM32X1

Primitive: 32-Deep by 1-Wide ROM



Introduction

This design element is a 32-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 5-bit address (A4 – A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of eight hexadecimal digits that are written into the ROM from the most-significant digit A=1FH to the least-significant digit A=00H.

For example, the INIT=10A78F39 parameter produces the data stream: 0001 0000 1010 0111 1000 1111 0011 1001. An error occurs if the INIT=value is not specified.

Logic Table

Input				Output
I0	I1	I2	I3	O
0	0	0	0	INIT(0)
0	0	0	1	INIT(1)
0	0	1	0	INIT(2)
0	0	1	1	INIT(3)
0	1	0	0	INIT(4)
0	1	0	1	INIT(5)
0	1	1	0	INIT(6)
0	1	1	1	INIT(7)
1	0	0	0	INIT(8)
1	0	0	1	INIT(9)
1	0	1	0	INIT(10)
1	0	1	1	INIT(11)
1	1	0	0	INIT(12)
1	1	0	1	INIT(13)
1	1	1	0	INIT(14)
1	1	1	1	INIT(15)

Design Entry Method

This design element can be used in schematics.

Available Attributes

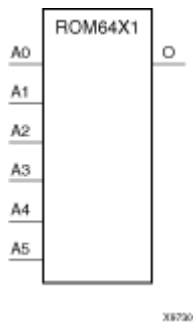
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 32-Bit Value	All zeros	Specifies the contents of the ROM.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

ROM64X1

Primitive: 64-Deep by 1-Wide ROM



Introduction

This design element is a 64-word by 1-bit read-only memory. The data output (O) reflects the word selected by the 6-bit address (A5 – A0). The ROM is initialized to a known value during configuration with the INIT=value parameter. The value consists of 16 hexadecimal digits that are written into the ROM from the most-significant digit A=FH to the least-significant digit A=0H. An error occurs if the INIT=value is not specified.

Logic Table

Input				Output
I0	I1	I2	I3	O
0	0	0	0	INIT(0)
0	0	0	1	INIT(1)
0	0	1	0	INIT(2)
0	0	1	1	INIT(3)
0	1	0	0	INIT(4)
0	1	0	1	INIT(5)
0	1	1	0	INIT(6)
0	1	1	1	INIT(7)
1	0	0	0	INIT(8)
1	0	0	1	INIT(9)
1	0	1	0	INIT(10)
1	0	1	1	INIT(11)
1	1	0	0	INIT(12)
1	1	0	1	INIT(13)
1	1	1	0	INIT(14)
1	1	1	1	INIT(15)

Design Entry Method

This design element can be used in schematics.

Available Attributes

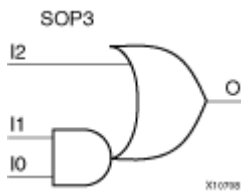
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 64-Bit Value	All zeros	Specifies the contents of the ROM.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SOP3

Macro: Sum of Products



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

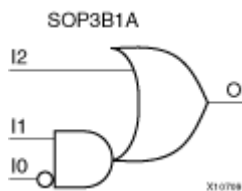
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SOP3B1A

Macro: Sum of Products



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

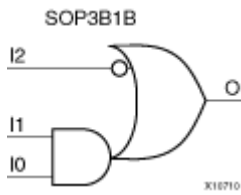
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SOP3B1B

Macro: Sum of Products



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

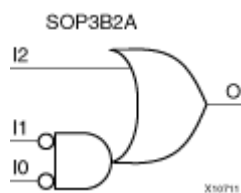
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SOP3B2A

Macro: Sum of Products



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

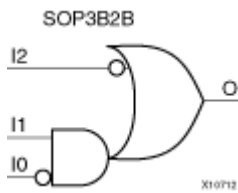
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SOP3B2B

Macro: Sum of Products



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

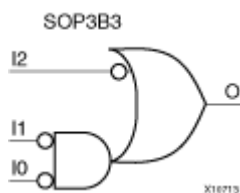
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SOP3B3

Macro: Sum of Products



Introduction

Three input Sum of Products (SOP) macros provide common logic functions by OR gating the output of one AND function with one direct input. Variations of inverting and non-inverting inputs are available.

Design Entry Method

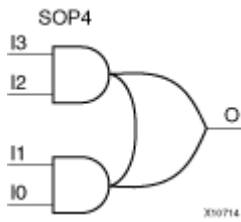
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SOP4

Macro: Sum of Products



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

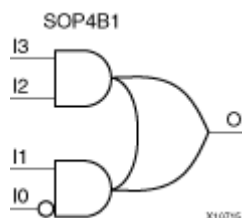
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SOP4B1

Macro: Sum of Products



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

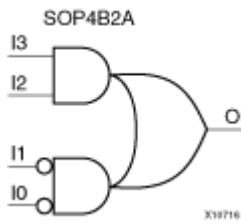
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SOP4B2A

Macro: Sum of Products



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

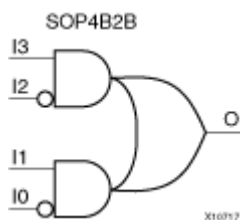
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SOP4B2B

Macro: Sum of Products



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

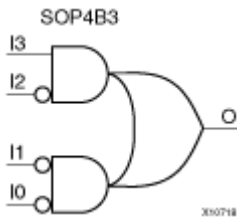
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SOP4B3

Macro: Sum of Products



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

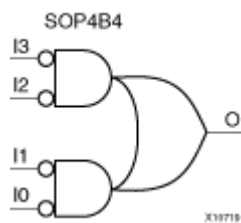
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SOP4B4

Macro: Sum of Products



Introduction

Four input Sum of Products (SOP) macros provide common logic functions by OR gating the outputs of two AND functions. Variations of inverting and non-inverting inputs are available.

Design Entry Method

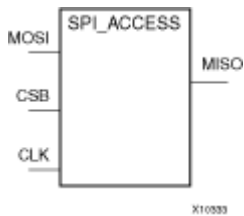
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SPI_ACCESS

Primitive: Internal Logic Access to the Serial Peripheral Interface (SPI) PROM Data



Introduction

This design element allows connection from the internal logic of the FPGA to an In-System Flash (ISF) Memory contained within the Spartan-3AN devices through an SPI serial protocol.

Port Descriptions

Name	Direction	Width	Function
MISO	Output	1-bit	Serial output data from the ISF Memory.
MOSI	Input	1-bit	Serial input instructions/data to the ISF Memory.
CSB	Input	1-bit	ISF Memory enable.
CLK	Input	1-bit	ISF Memory clock.

Design Entry Method

This design element can be used in schematics.

Available Attributes

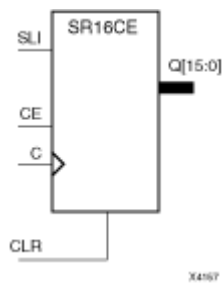
Attribute	Type	Allowed Values	Default	Description
SIM_DEVICE	String	3S50AN, 3S200AN, 3S400AN, 3S700AN or 3S1400AN	"UNSPECIFIED"	Specifies the target device so that the proper size ISF Memory is used. This attribute <i>must</i> be set.
SIM_USER_ID	64-bit Hex Value	Any 64-bit Hex Value	All locations default to 0xFF	Specifies the programmed USER ID in the Security Register for the ISF Memory.
SIM_MEM_FILE	String	Specified file and directory name.	"NONE"	Optionally specifies a hex file containing the initialization memory content for the ISF Memory.
SIM_FACTORY_ID	64-bit Hex Value	Any 64-bit Hex Value	All locations default to 0xFF	Specifies the Unique Identifier value in the Security Register for simulation purposes (the actual HW value will be specific to the particular device used).
SIM_DELAY_TYPE	String	"ACCURATE", "SCALED"	"SCALED"	Scales down some timing delays for faster simulation run. "ACCURATE" = timing and delays consistent with datasheet specs. "SCALED" = timing numbers scaled back to run faster simulation, behavior not affected.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SR16CE

Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel outputs (Q), and clock enable (CE) and asynchronous clear (CLR) inputs. The (CLR) input, when High, overrides all other inputs and resets the data outputs (Q) Low. When (CE) is High and (CLR) is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and (CLR) is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI→Q0, Q0→Q1, Q1→Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (CLR) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs	
CLR	CE	SLI	C	Q0	Qz - Q1
1	X	X	X	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1

z = bit width - 1
qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

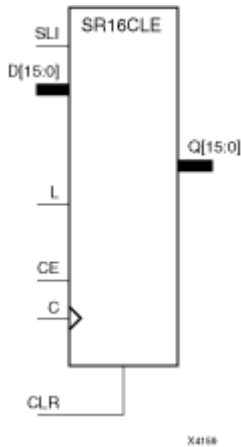
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SR16CLE

Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR). The register ignores clock transitions when (L) and (CE) are Low. The asynchronous (CLR), when High, overrides all other inputs and resets the data outputs (Q) Low. When (L) is High and (CLR) is Low, data on the Dn – D0 inputs is loaded into the corresponding Qn – (Q0) bits of the register.

When (CE) is High and (L) and (CLR) are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent clock transitions, when (CE) is High and (L) and (CLR) are Low, the data shifts to the next highest bit position as new data is loaded into (Q)0 (for example, SLI→Q0, Q0→Q1, and Q1→Q2).

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (CLR) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs						Outputs	
CLR	L	CE	SLI	Dn – D0	C	Q0	Qz – Q1
1	X	X	X	X	X	0	0
0	1	X	X	Dn – D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change

z = bitwidth -1

qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

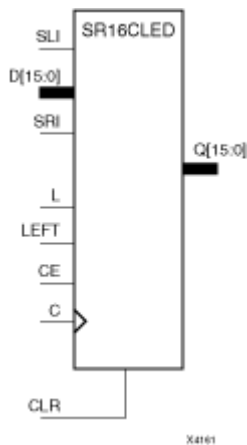
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SR16CLED

Macro: 16-Bit Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when (CE) and (L) are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low.

When (L) is High and (CLR) is Low, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register. When (CE) is High and (L) and (CLR) are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 or Q2) during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last (Q) output during the Low-to-High clock transition and shifted right during subsequent clock transitions. The logic tables indicate the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs								Outputs		
CLR	L	CE	LEFT	SLI	SRI	D15 – D0	C	Q0	Q15	Q14 – Q1
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D15 – D0	↑	D0	D15	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q14	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition.

Design Entry Method

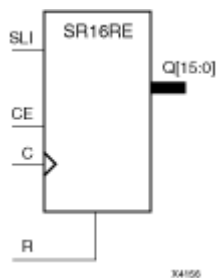
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SR16RE

Macro: 16-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low.

When (CE) is High and (R) is Low, the data on the (SLI) is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and R is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (for example, SLI→Q0, Q0→Q1, and Q1→Q2). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (R) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs	
R	CE	SLI	C	Q0	Qz - Q1
1	X	X	↑	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1

z = bitwidth -1
qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

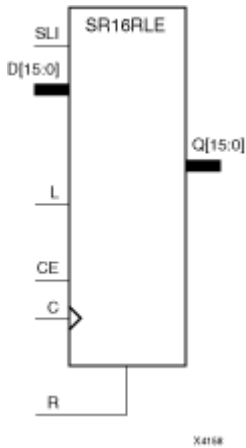
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SR16RLE

Macro: 16-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when (L) and (CE) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, data on the (D) inputs is loaded into the corresponding Q bits of the register.

When (CE) is High and (L) and (R) are Low, data on the (SLI) input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when (CE) is High and (L) and (R) are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (R) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs						Outputs	
R	L	CE	SLI	Dz - D0	C	Q0	Qz - Q1
1	X	X	X	X	↑	0	0
0	1	X	X	Dz - D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1							
qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

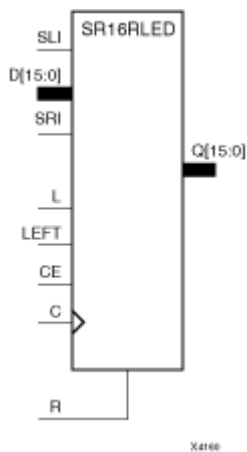
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SR16RLED

Macro: 16-Bit Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q) and four control inputs — clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when (CE) and (L) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register.

When (CE) is High and (L) and (R) are Low, data shifts right or left, depending on the state of the LEFT input. If LEFT is High, data on (SLI) is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 and Q2) during subsequent clock transitions. If LEFT is Low, data on the (SRI) is loaded into the last (Q) output during the Low-to-High clock transition and shifted right) during subsequent clock transitions. The logic tables below indicates the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs								Outputs		
R	L	CE	LEFT	SLI	SRI	D15 – D0	C	Q0	Q15	Q14 – Q1
1	X	X	X	X	X	X	↑	0	0	0
0	1	X	X	X	X	D15 – D0	↑	D0	D15	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q14	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

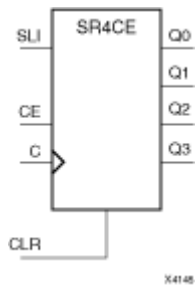
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SR4CE

Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel outputs (Q), and clock enable (CE) and asynchronous clear (CLR) inputs. The (CLR) input, when High, overrides all other inputs and resets the data outputs (Q) Low. When (CE) is High and (CLR) is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and (CLR) is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI→Q0, Q0→Q1, Q1→Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (CLR) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs	
CLR	CE	SLI	C	Q0	Qz - Q1
1	X	X	X	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1

z = bit width - 1
qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

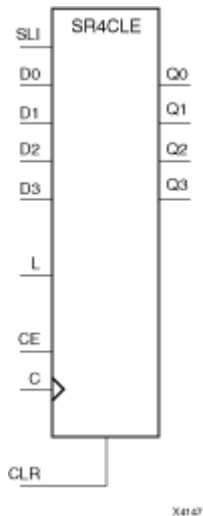
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SR4CLE

Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR). The register ignores clock transitions when (L) and (CE) are Low. The asynchronous (CLR), when High, overrides all other inputs and resets the data outputs (Q) Low. When (L) is High and (CLR) is Low, data on the Dn – D0 inputs is loaded into the corresponding Qn – (Q0) bits of the register.

When (CE) is High and (L) and (CLR) are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent clock transitions, when (CE) is High and (L) and (CLR) are Low, the data shifts to the next highest bit position as new data is loaded into (Q)0 (for example, SLI→Q0, Q0→Q1, and Q1→Q2).

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (CLR) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs						Outputs	
CLR	L	CE	SLI	Dn – D0	C	Q0	Qz – Q1
1	X	X	X	X	X	0	0
0	1	X	X	Dn – D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change

z = bitwidth -1

qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

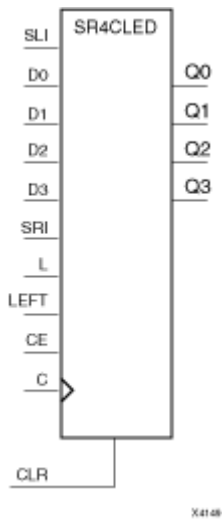
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SR4CLED

Macro: 4-Bit Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when (CE) and (L) are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low.

When (L) is High and (CLR) is Low, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register. When (CE) is High and (L) and (CLR) are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 or Q2) during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last (Q) output during the Low-to-High clock transition and shifted right during subsequent clock transitions. The logic tables indicate the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs								Outputs		
CLR	L	CE	LEFT	SLI	SRI	D3 – D0	C	Q0	Q3	Q2 – Q1
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D3– D0	↑	D0	D3	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q2	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1

qn-1 and qn+1 = state of referenced output one setup time prior to active clock transition.

Design Entry Method

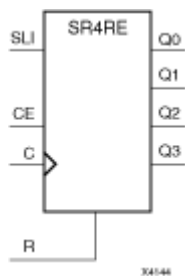
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SR4RE

Macro: 4-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low.

When (CE) is High and (R) is Low, the data on the (SLI) is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and R is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (for example, SLI→Q0, Q0→Q1, and Q1→Q2). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (R) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs				Outputs	
R	CE	SLI	C	Q0	Qz - Q1
1	X	X	↑	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1

z = bitwidth -1
qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

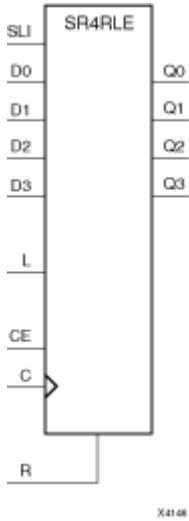
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SR4RLE

Macro: 4-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when (L) and (CE) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, data on the (D) inputs is loaded into the corresponding Q bits of the register.

When (CE) is High and (L) and (R) are Low, data on the (SLI) input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when (CE) is High and (L) and (R) are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (R) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs						Outputs	
R	L	CE	SLI	Dz – D0	C	Q0	Qz – Q1
1	X	X	X	X	↑	0	0
0	1	X	X	Dz – D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1							
qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

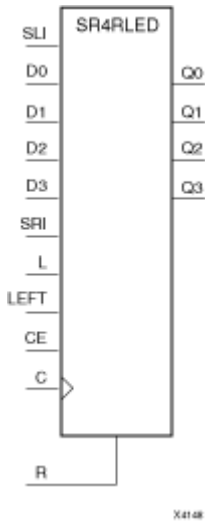
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SR4RLED

Macro: 4-Bit Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q) and four control inputs — clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when (CE) and (L) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register.

When (CE) is High and (L) and (R) are Low, data shifts right or left, depending on the state of the LEFT input. If LEFT is High, data on (SLI) is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 and Q2) during subsequent clock transitions. If LEFT is Low, data on the (SRI) is loaded into the last (Q) output during the Low-to-High clock transition and shifted right) during subsequent clock transitions. The logic tables below indicates the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs								Outputs		
R	L	CE	LEFT	SLI	SRI	D3 – D0	C	Q0	Q3	Q2 – Q1
1	X	X	X	X	X	X	↑	0	0	0
0	1	X	X	X	X	D3 – D0	↑	D0	D3	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q2	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

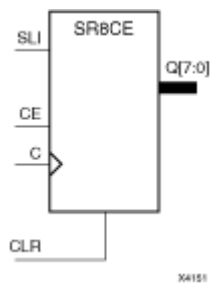
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SR8CE

Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel outputs (Q), and clock enable (CE) and asynchronous clear (CLR) inputs. The (CLR) input, when High, overrides all other inputs and resets the data outputs (Q) Low. When (CE) is High and (CLR) is Low, the data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and (CLR) is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (SLI→Q0, Q0→Q1, Q1→Q2, and so forth). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (CLR) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs	
CLR	CE	SLI	C	Q0	Qz - Q1
1	X	X	X	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1

z = bit width - 1
qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

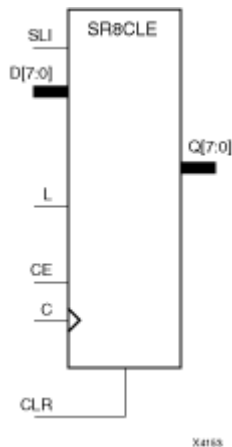
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SR8CLE

Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with a shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and asynchronous clear (CLR). The register ignores clock transitions when (L) and (CE) are Low. The asynchronous (CLR), when High, overrides all other inputs and resets the data outputs (Q) Low. When (L) is High and (CLR) is Low, data on the $D_n - D_0$ inputs is loaded into the corresponding $Q_n - (Q_0)$ bits of the register.

When (CE) is High and (L) and (CLR) are Low, data on the SLI input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent clock transitions, when (CE) is High and (L) and (CLR) are Low, the data shifts to the next highest bit position as new data is loaded into (Q)0 (for example, $SLI \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, and $Q_1 \rightarrow Q_2$).

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (CLR) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs						Outputs	
CLR	L	CE	SLI	$D_n - D_0$	C	Q0	$Q_z - Q_1$
1	X	X	X	X	X	0	0
0	1	X	X	$D_n - D_0$	↑	D0	D_n
0	0	1	SLI	X	↑	SLI	q_{n-1}
0	0	0	X	X	X	No Change	No Change

$z = \text{bitwidth} - 1$

q_{n-1} = state of referenced output one setup time prior to active clock transition

Design Entry Method

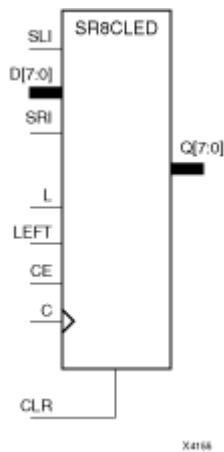
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SR8CLED

Macro: 8-Bit Shift Register with Clock Enable and Asynchronous Clear



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q), and four control inputs: clock enable (CE), load enable (L), shift left/right (LEFT), and asynchronous clear (CLR). The register ignores clock transitions when (CE) and (L) are Low. The asynchronous clear, when High, overrides all other inputs and resets the data outputs (Qn) Low.

When (L) is High and (CLR) is Low, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register. When (CE) is High and (L) and (CLR) are Low, data is shifted right or left, depending on the state of the LEFT input. If LEFT is High, data on the SLI is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 or Q2) during subsequent clock transitions. If LEFT is Low, data on the SRI is loaded into the last (Q) output during the Low-to-High clock transition and shifted right during subsequent clock transitions. The logic tables indicate the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs								Outputs		
CLR	L	CE	LEFT	SLI	SRI	D7 – D0	C	Q0	Q7	Q6 – Q1
1	X	X	X	X	X	X	X	0	0	0
0	1	X	X	X	X	D7 – D0	↑	D0	D7	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q6	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1

qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition.

Design Entry Method

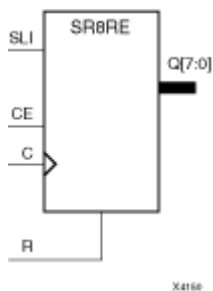
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SR8RE

Macro: 8-Bit Serial-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel outputs (Qn), clock enable (CE), and synchronous reset (R) inputs. The R input, when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low.

When (CE) is High and (R) is Low, the data on the (SLI) is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the (Q0) output. During subsequent Low-to-High clock transitions, when (CE) is High and R is Low, data shifts to the next highest bit position as new data is loaded into (Q0) (for example, SLI→Q0, Q0→Q1, and Q1→Q2). The register ignores clock transitions when (CE) is Low.

Registers can be cascaded by connecting the last (Q) output of one stage to the SLI input of the next stage and connecting clock, (CE), and (R) in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate `STARTUP_architecture` symbol.

Logic Table

Inputs				Outputs	
R	CE	SLI	C	Q0	Qz - Q1
1	X	X	↑	0	0
0	0	X	X	No Change	No Change
0	1	SLI	↑	SLI	qn-1

z = bitwidth -1
qn-1 = state of referenced output one setup time prior to active clock transition

Design Entry Method

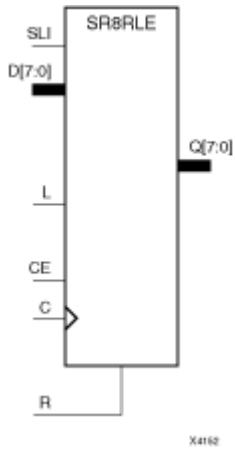
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SR8RLE

Macro: 8-Bit Loadable Serial/Parallel-In Parallel-Out Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left serial input (SLI), parallel inputs (D), parallel outputs (Q), and three control inputs: clock enable (CE), load enable (L), and synchronous reset (R). The register ignores clock transitions when (L) and (CE) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, data on the (D) inputs is loaded into the corresponding Q bits of the register.

When (CE) is High and (L) and (R) are Low, data on the (SLI) input is loaded into the first bit of the shift register during the Low-to-High clock (C) transition and appears on the Q0 output. During subsequent clock transitions, when (CE) is High and (L) and (R) are Low, the data shifts to the next highest bit position as new data is loaded into Q0.

Registers can be cascaded by connecting the last Q output of one stage to the SLI input of the next stage and connecting clock, (CE), (L), and (R) inputs in parallel.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate *STARTUP_architecture* symbol.

Logic Table

Inputs						Outputs	
R	L	CE	SLI	Dz - D0	C	Q0	Qz - Q1
1	X	X	X	X	↑	0	0
0	1	X	X	Dz - D0	↑	D0	Dn
0	0	1	SLI	X	↑	SLI	qn-1
0	0	0	X	X	X	No Change	No Change
z = bitwidth -1							
qn-1 = state of referenced output one setup time prior to active clock transition							

Design Entry Method

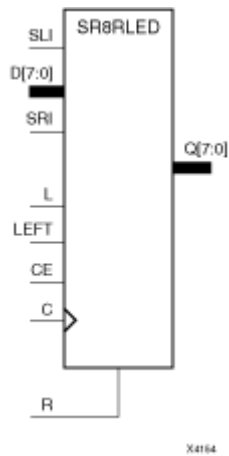
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SR8RLED

Macro: 8-Bit Shift Register with Clock Enable and Synchronous Reset



Introduction

This design element is a shift register with shift-left (SLI) and shift-right (SRI) serial inputs, parallel inputs (D), parallel outputs (Q) and four control inputs — clock enable (CE), load enable (L), shift left/right (LEFT), and synchronous reset (R). The register ignores clock transitions when (CE) and (L) are Low. The synchronous (R), when High, overrides all other inputs during the Low-to-High clock (C) transition and resets the data outputs (Q) Low. When (L) is High and (R) is Low during the Low-to-High clock transition, the data on the (D) inputs is loaded into the corresponding (Q) bits of the register.

When (CE) is High and (L) and (R) are Low, data shifts right or left, depending on the state of the LEFT input. If LEFT is High, data on (SLI) is loaded into (Q0) during the Low-to-High clock transition and shifted left (for example, to Q1 and Q2) during subsequent clock transitions. If LEFT is Low, data on the (SRI) is loaded into the last (Q) output during the Low-to-High clock transition and shifted right) during subsequent clock transitions. The logic tables below indicates the state of the (Q) outputs under all input conditions.

This register is asynchronously cleared, outputs Low, when power is applied. For FPGA devices, power-on conditions are simulated when global set/reset (GSR) is active. GSR defaults to active-High but can be inverted by adding an inverter in front of the GSR input of the appropriate STARTUP_architecture symbol.

Logic Table

Inputs								Outputs		
R	L	CE	LEFT	SLI	SRI	D7- D0	C	Q0	Q7	Q6 - Q1
1	X	X	X	X	X	X	↑	0	0	0
0	1	X	X	X	X	D7 - D0	↑	D0	D7	Dn
0	0	0	X	X	X	X	X	No Change	No Change	No Change
0	0	1	1	SLI	X	X	↑	SLI	q6	qn-1
0	0	1	0	X	SRI	X	↑	q1	SRI	qn+1
qn-1 or qn+1 = state of referenced output one setup time prior to active clock transition										

Design Entry Method

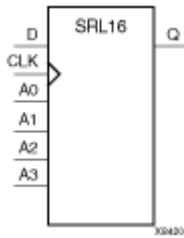
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SRL16

Primitive: 16-Bit Shift Register Look-Up-Table (LUT)



Introduction

This design element is a shift register look-up table (LUT). The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register** - Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: $\text{Length} = (8 \times A3) + (4 \times A2) + (2 \times A1) + A0 + 1$. If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically** - Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The data (D) is loaded into the first bit of the shift register during the Low-to-High clock (CLK) transition. During subsequent Low-to-High clock transitions data shifts to the next highest bit position while new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

Logic Table

Inputs			Output
A _m	CLK	D	Q
A _m	X	X	Q(A _m)
A _m	↑	D	Q(A _m - 1)
m = 0, 1, 2, 3			

Design Entry Method

This design element can be used in schematics.

Available Attributes

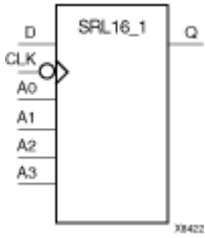
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of Q output after configuration.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SRL16_1

Primitive: 16-Bit Shift Register Look-Up-Table (LUT) with Negative-Edge Clock



Introduction

This design element is a shift register look-up table (LUT). The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register** - Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: $\text{Length} = (8 \times A3) + (4 \times A2) + (2 \times A1) + A0 + 1$. If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically** - Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The data (D) is loaded into the first bit of the shift register during the High-to-Low clock (CLK) transition. During subsequent High-to-Low clock transitions data shifts to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

Logic Table

Inputs			Output
A _m	CLK	D	Q
A _m	X	X	Q(A _m)
A _m	↓	D	Q(A _m - 1)
m = 0, 1, 2, 3			

Design Entry Method

This design element can be used in schematics.

Available Attributes

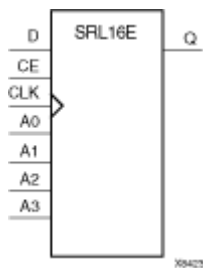
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of Q output after configuration

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SRL16E

Primitive: 16-Bit Shift Register Look-Up-Table (LUT) with Clock Enable



Introduction

This design element is a shift register look-up table (LUT). The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- To create a fixed-length shift register** - Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: $\text{Length} = (8 \times A3) + (4 \times A2) + (2 \times A1) + A0 + 1$. If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- To change the length of the shift register dynamically** - Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

When CE is High, the data (D) is loaded into the first bit of the shift register during the Low-to-High clock (CLK) transition. During subsequent Low-to-High clock transitions, when CE is High, data shifts to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached. When CE is Low, the register ignores clock transitions.

Logic Table

Inputs				Output
A _m	CE	CLK	D	Q
A _m	0	X	X	Q(A _m)
A _m	1	↑	D	Q(A _m - 1)
m = 0, 1, 2, 3				

Design Entry Method

This design element can be used in schematics.

Available Attributes

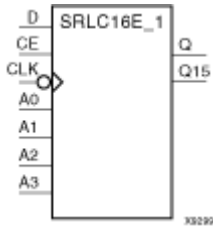
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SRL16E_1

Primitive: 16-Bit Shift Register Look-Up-Table (LUT) with Negative-Edge Clock and Clock Enable



Introduction

This design element is a shift register look up table (LUT) with clock enable (CE). The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register** - Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: $\text{Length} = (8 \times A3) + (4 \times A2) + (2 \times A1) + A0 + 1$. If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically** - Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

When CE is High, the data (D) is loaded into the first bit of the shift register during the High-to-Low clock (CLK) transition. During subsequent High-to-Low clock transitions, when CE is High, data is shifted to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached. When CE is Low, the register ignores clock transitions.

Logic Table

Inputs				Output
A _m	CE	CLK	D	Q
A _m	0	X	X	Q(A _m)
A _m	1	↓	D	Q(A _m - 1)
m = 0, 1, 2, 3				

Design Entry Method

This design element can be used in schematics.

Available Attributes

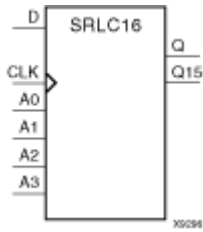
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	16-Bit Hexadecimal	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SRLC16

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry



Introduction

This design element is a shift register look-up table (LUT) with Carry. The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register** - Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: $\text{Length} = (8 \times A3) + (4 \times A2) + (2 \times A1) + A0 + 1$. If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically** - Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The data (D) is loaded into the first bit of the shift register during the Low-to-High clock (CLK) transition. During subsequent Low-to-High clock transitions data shifts to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached. The Q15 output is available for you in cascading to multiple shift register LUTs to create larger shift registers.

Logic Table

Inputs			Output
A _m	CLK	D	Q
A _m	X	X	Q(A _m)
A _m	↑	D	Q(A _m - 1)
m = 0, 1, 2, 3			

Design Entry Method

This design element can be used in schematics.

Available Attributes

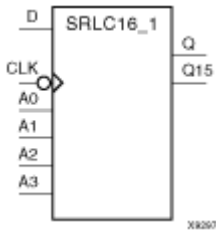
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SRLC16_1

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry and Negative-Edge Clock



Introduction

This design element is a shift register look-up table (LUT) with carry and a negative-edge clock. The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- To create a fixed-length shift register** - Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: $\text{Length} = (8 \times A3) + (4 \times A2) + (2 \times A1) + A0 + 1$. If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- To change the length of the shift register dynamically** - Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The Q15 output is available for your use in cascading multiple shift register LUTs to create larger shift registers.

Logic Table

Inputs			Output	
A _m	CLK	D	Q	Q15
A _m	X	X	Q(A _m)	No Change
A _m	↓	D	Q(A _m - 1)	Q14
m = 0, 1, 2, 3				

Design Entry Method

This design element can be used in schematics.

Available Attributes

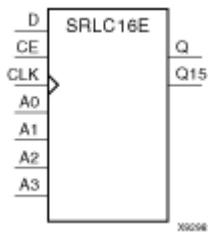
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SRLC16E

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry and Clock Enable



Introduction

This design element is a shift register look-up table (LUT) with carry and clock enable. The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- To create a fixed-length shift register** - Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: $\text{Length} = (8 \times A3) + (4 \times A2) + (2 \times A1) + A0 + 1$. If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- To change the length of the shift register dynamically** - Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

The data (D) is loaded into the first bit of the shift register during the Low-to-High clock (CLK) transition. When CE is High, during subsequent Low-to-High clock transitions, data shifts to the next highest bit position as new data is loaded. The data appears on the Q output when the shift register length determined by the address inputs is reached.

The Q15 output is available for you in cascading to multiple shift register LUTs to create larger shift registers.

Logic Table

Inputs				Output	
Am	CLK	CE	D	Q	Q15
Am	X	0	X	Q(Am)	Q(15)
Am	X	1	X	Q(Am)	Q(15)
Am	↑	1	D	Q(Am - 1)	Q15
m = 0, 1, 2, 3					

Design Entry Method

This design element can be used in schematics.

Available Attributes

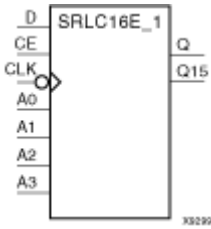
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

SRLC16E_1

Primitive: 16-Bit Shift Register Look-Up Table (LUT) with Carry, Negative-Edge Clock, and Clock Enable



Introduction

This design element is a shift register look-up table (LUT) with carry, clock enable, and negative-edge clock. The inputs A3, A2, A1, and A0 select the output length of the shift register.

The shift register can be of a fixed, static length or it can be dynamically adjusted.

- **To create a fixed-length shift register** - Drive the A3 through A0 inputs with static values. The length of the shift register can vary from 1 bit to 16 bits, as determined by the following formula: $Length = (8 \times A3) + (4 \times A2) + (2 \times A1) + A0 + 1$. If A3, A2, A1, and A0 are all zeros (0000), the shift register is one bit long. If they are all ones (1111), it is 16 bits long.
- **To change the length of the shift register dynamically** - Change the values driving the A3 through A0 inputs. For example, if A2, A1, and A0 are all ones (111) and A3 toggles between a one (1) and a zero (0), the length of the shift register changes from 16 bits to 8 bits. Internally, the length of the shift register is always 16 bits and the input lines A3 through A0 select which of the 16 bits reach the output.

The shift register LUT contents are initialized by assigning a four-digit hexadecimal number to an INIT attribute. The first, or the left-most, hexadecimal digit is the most significant bit. If an INIT value is not specified, it defaults to a value of four zeros (0000) so that the shift register LUT is cleared during configuration.

When CE is High, the data (D) is loaded into the first bit of the shift register during the High-to-Low clock (CLK) transition. During subsequent High-to-Low clock transitions data shifts to the next highest bit position as new data is loaded when CE is High. The data appears on the Q output when the shift register length determined by the address inputs is reached.

The Q15 output is available for your use in cascading multiple shift register LUTs to create larger shift registers.

Logic Table

Inputs				Output	
A _m	CE	CLK	D	Q	Q15
A _m	0	X	X	Q(A _m)	No Change
A _m	1	X	X	Q(A _m)	No Change
A _m	1	↓	D	Q(A _m - 1)	Q14
m = 0, 1, 2, 3					

Design Entry Method

This design element can be used in schematics.

Available Attributes

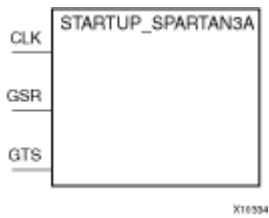
Attribute	Type	Allowed Values	Default	Description
INIT	Hexadecimal	Any 16-Bit Value	All zeros	Sets the initial value of content and output of shift register after configuration.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

STARTUP_SPARTAN3A

Primitive: Spartan-3A Global Set/Reset, Global 3-State and Configuration Start-Up Clock Interface



Introduction

This design element is used to either interface device pins and logic to the global asynchronous set/reset (GSR) signal, or for global, 3-state (GTS) dedicated routing. This primitive can also be used to specify a different clock for the device startup sequence at the end of configuring the device.

Port Descriptions

Name	Direction	Width	Function
GSR	Input	1-bit	Input connection to the global set / reset (GSR) routing.
GTS	Input	1-bit	Input connection to the global 3-state (GTS) routing.
CLK	Input	1-bit	Input connection to the configuration startup sequence clock (GSR) routing.

Design Entry Method

This design element can be used in schematics.

To use the dedicated GSR circuitry, connect the sourcing pin or logic to the GSR pin. However, avoid using the GSR circuitry of this component unless certain precautions are taken first. Since the skew of the GSR net cannot be guaranteed, either use general routing for the set/reset signal in which routing delays and skew can be calculated as a part of the timing analysis of the design or to take preventative measures to ensure that possible skew on the release of the clock cycle won't interfere with circuit operation.

Similarly, if the dedicated global 3-state is used, connect the appropriate sourcing pin or logic to the GTS input pin of the primitive. In order to specify a clock for the startup sequence of configuration, connect a clock from the design to the CLK pin of this design element.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

VCC

Primitive: VCC-Connection Signal Tag



Introduction

This design element serves as a signal tag, or parameter, that forces a net or input function to a logic High level. A net tied to this element cannot have any other source.

When the placement and routing software encounters a net or input function tied to this element, it removes any logic that is disabled by the Vcc signal, which is only implemented when the disabled logic cannot be removed.

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

XNOR2

Primitive: 2-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

XNOR3

Primitive: 3-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

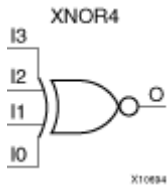
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

XNOR4

Primitive: 4-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

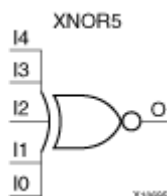
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

XNOR5

Primitive: 5-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

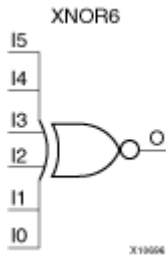
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

XNOR6

Macro: 6-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

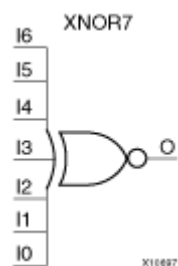
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

XNOR7

Macro: 7-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

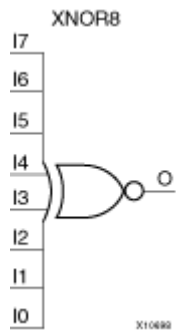
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

XNOR8

Macro: 8-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

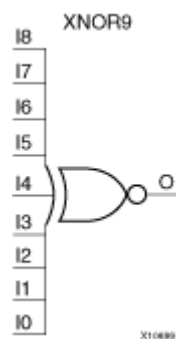
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

XNOR9

Macro: 9-Input XNOR Gate with Non-Inverted Inputs



Introduction

XNOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Logic Table

Input	Output
I0 ... Iz	O
Odd number of 1	0
Even number of 1	1

Design Entry Method

This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

XOR2

Primitive: 2-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

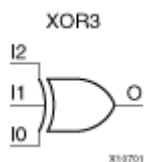
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

XOR3

Primitive: 3-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

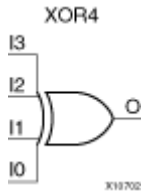
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

XOR4

Primitive: 4-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

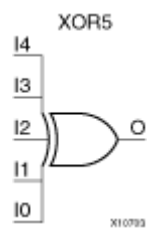
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

XOR5

Primitive: 5-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

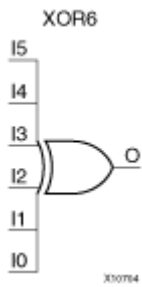
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

XOR6

Macro: 6-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

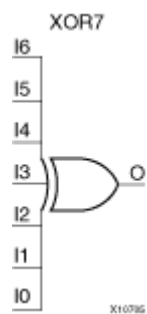
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

XOR7

Macro: 7-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

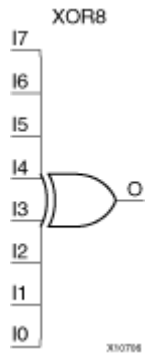
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

XOR8

Macro: 8-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

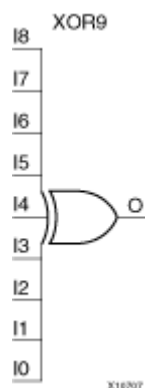
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

XOR9

Macro: 9-Input XOR Gate with Non-Inverted Inputs



Introduction

XOR functions of up to nine inputs are available. All inputs are non-inverting. Because each input uses a CLB resource, replace functions with unused inputs with functions having the necessary number of inputs.

Design Entry Method

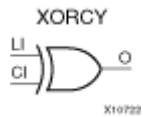
This design element is only for use in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

XORCY

Primitive: XOR for Carry Logic with General Output



Introduction

This design element is a special XOR with general O output that generates faster and smaller arithmetic functions. The XORCY primitive is a dedicated XOR function within the carry-chain logic of the slice. It allows for fast and efficient creation of arithmetic (add/subtract) or wide logic functions (large AND/OR gate).

Logic Table

Input		Output
LI	CI	O
0	0	0
0	1	1
1	0	1
1	1	0

Design Entry Method

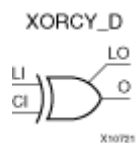
This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

XORCY_D

Primitive: XOR for Carry Logic with Dual Output



Introduction

This design element is a special XOR that generates faster and smaller arithmetic functions.

Logic Table

Input		Output
LI	CI	O and LO
0	0	0
0	1	1
1	0	1
1	1	0

Design Entry Method

This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).

XORCY_L

Primitive: XOR for Carry Logic with Local Output



Introduction

This design element is a special XOR with local LO output that generates faster and smaller arithmetic functions.

Logic Table

Input		Output
LI	CI	LO
0	0	0
0	1	1
1	0	1
1	1	0

Design Entry Method

This design element can be used in schematics.

For More Information

- See the [Spartan-3A User Guide](#).
- See the [Spartan-3A Data Sheets](#).