Sample Curriculum for a one-semester introductory course in Digital Logic, assuming three lectures per week and one lab session per week

Lecture number	Topics covered	Textbook sections *	Quartus II Tutorials and Lab Exercises
1	Overview of the course: topics covered, mark assignments (midterm test, labs, final exam), quick overview of digital systems and Moore's law, examples of digital systems, overview of how the lab exercises are organized (students work in small groups (two per group?), marks assigned for preparation and lab performance); short introduction to the DE2 board (its FPGA can be used to implement any digital circuit that fits in this chip, it has lots of useful I/O features)	Chapter 1	
2	Transistors as simple on-off switches; introduction to logic expressions; AND, OR, NOT circuits built using switches; AND, OR, NOT gate symbols; truth tables; simple example of logic circuit with AND, OR, NOT gates	2.1 - 2.4	
3	Boolean algebra: duality, axioms, rules, identities; proof of identities using perfect induction (i.e., truth tables); algebraic manipulation of Boolean expressions; timing diagrams; Venn Diagrams and their use to prove some identities	2.5	
4	Simple synthesis of logic circuits; sum-of-products (SOP) form; minterms; canonical SOP; product-of-sums form (POS); maxterms; canonical POS; examples of algebraic manipulation	2.6	**Tutorial: Getting Started with the DE2 Board** **Tutorial: Introduction to Quartus II using Schematic Entry** (Perform the tutorial steps in the lab; use the DE2 board)
5	Example logic functions: 2-to-1 multiplexer, XOR gate; NAND and NOR logic networks; convert SOP to NAND-NAND, POS to NOR-NOR	2.7	
6	Binary numbers; full adder, ripple-carry adder	5.1 - 5.2	
7	Introduction to CAD tools; introduction to VHDL/Verilog; introduction to Field Programmable Gate Arrays (FPGAs)	2.9, 3.6	**Tutorial: Introduction to Quartus II using Verilog/VHDL** (Perform the tutorial steps outside the lab; use simulation only) **Lab 1: Lights, Switches, and Multiplexers**
8	Introduction to cost of a logic circuit; terminology: implicant, prime implicant (PI), essential PI, cover, minimum-cost cover; introduction to K-maps (2, 3, 4 variables)	4.1 - 4.3	
9	5-variable K-maps; don't cares, and examples; 7-seg example	4.1 - 4.4	
10	Spare lecture (for review, etc)		**Lab 2: Numbers and Displays**
11	Storage elements: introduction, RS latches, timing diagrams, gated RS latch	7.1 - 7.2	
12	Gated D latch, D flip-flops, setup and hold times	7.3 - 7.4	
13	Flip-flop reset/preset; registers; shift registers; parallel load; flip-flop timing	7.4 - 7.8	**Lab 3: Latches, Flip-flops, and Registers**
14	Counters; ripple and synchronous counters	7.9 - 7.11	
15	VHDL/Verilog code for synchronous circuits	7.12 - 7.14	
16	Signed numbers; 2's complement; adders/subtractors	5.3	**Lab 4: Counters**
17	Multipliers	5.6	
18	Combinational circuits: implementing logic functions using only multiplexers	6.1 - 6.3	
19	Decoders, encoders, code converters, comparators; VHDL/Verilog	6.4 - 6.6	**Lab 5: Clocks and Timers**
20	Spare lecture (for review, etc)		
21	Timing analysis of logic circuits		
22	Finite state machines introductions	8.1 - 8.5	**Tutorial: Using the Library of Parameterized Modules** **Tutorial: Timing Considerations** **Tutorial: Quartus II Simulation** **Lab 6: Adders, Subtractors, and Multipliers**
23	FSM state assignment	8.1 - 8.5	
24	FSM timing issues (Moore and Mealy models); Verilog/VHDL code	8.1 - 8.5	
25	State minimization	8.6	**Lab 7: Finite State Machines**
26	Introduction to SRAM	10.1	
27	SRAM blocks in an FPGA	10.1, 10.3	
28	Design example: introduction to Processors	7.14	**Lab 8: Memory Blocks ****
29	Design example: introduction to Processors 2	7.14	
30	Spare lecture (for review, etc)		
31	Transistor circuits; building logic gates with transistors; CMOS	3.1 - 3.3	**Lab 9, 10: Processors ****
32	Speed of transistor circuits: propagation delay, rise/fall time, fanout	3.1 - 3.3	
33	Review and design examples		
34	Review and design examples		

* Stephen Brown and Zvonko Vranesic, McGraw Hill, **Fundamentals of Digital Logic with VHDL Design**, 2nd Edition, 915 pages, July 2004, or
* Stephen Brown and Zvonko Vranesic, McGraw Hill, **Fundamentals of Digital Logic with Verilog Design**, 1st Edition, 850 pages, June 2002

** Labs 8 - 10 could be replaced with a project of the student's choosing